

DIRECT AC CONTROL OF GRID ASSETS

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This dissertation is dedicated to my parents

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LIST OF SYMBOLS AND ABBREVIATIONS

D	duty cycle
K_0	DC component of D the duty cycle
K_2	magnitude of the second harmonic component of D
Φ_2	phase angle of the second harmonic component of D
K_4	magnitude of the fourth harmonic component of D
Φ_4	phase angle of the fourth harmonic component of D
V_3	magnitude of the third harmonic component
Φ_3	phase angle of the third harmonic component
VQS	virtual quadrature sources
STATCOM	static compensator
ILSTATCOM	inverter-less STATCOM
CNT	controllable network transformer
FACTS	flexible ac transmission systems
TACC	thin AC converter

SUMMARY

The objective of the proposed research is to investigate feasible approaches to dynamic control of the power grid. Growth in the demand for electric power and increase in the penetration of renewable energy resources is causing congestion on the power networks. The power grid is a constantly changing entity because of the dynamic nature of generation and loads. This makes the system very complex and extremely difficult to control. The primary parameters that need to be controlled are the voltage magnitude at every node in the system and the power flow in the network. Devices currently exist that are used on the networks to provide control of these parameters. Some of these devices include mechanically switched capacitors, load tap changing transformers, and more recently FACTS devices.

The resources available on the grid can be broadly classified as static and dynamic resources. Static resources are described as resources that can be used to provide scheduled support on the system. Mathematical tools such as load forecasting and load flow analyses are typically used to determine the set points for these resources. Static resources provide no support on the grid during unforeseen conditions such as faults or changes in generation patterns from sources like wind power. Dynamic resources can be used to control the system and help the system ride-through such conditions. Commercially available FACTS devices are an example of dynamic resources. These devices have however seen minimal market penetration because of high cost and poor reliability.

The proposed research aims at providing a low-cost solution to dynamic grid control. The approach uses existing static resources on the grid to provide dynamic control by augmenting the resources with a Thin AC Converter. The converter-augmented asset has a fail-normal mode of operation to ensure high system reliability, and is controlled using the concept of Virtual Quadrature Sources to realize enhanced control capabilities. This concept is a novel approach to single-phase ac power conversion with no bulk energy storage.

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

There is a growing need for dynamic control of the power system. The primary driving factors are the growth in penetration of renewable resources and growth in the consumption of power. The power system is operated with conservative safety margins. Dynamics seen on the network today do not impact the network significantly enough to cause interruption in supply of power to the consumer. This will however not be the case in the near future because of the decreasing safety margins with which the system is operated.

Resources used to control operation of the power system can be classified as static and dynamic. The classification is based on the steady state and dynamic control capabilities and response times. Along with the need for dynamic control, increased controllability of the power network is also desirable. This is required to ensure maximum utilization of the existing infrastructure.

Dynamic controllability of the network is achievable using commercially available solutions. These solutions are however cost intensive and have poor reliability, as they are typically single-point solutions, failure of which will result in large sections of the network being affected.

1.2 OBJECTIVE

The objective of the proposed research is to develop a low-cost solution to provide dynamic control in power networks. The goal is to leverage existing grid resources to provide the necessary control. This is achieved by augmenting the asset with a fractionally rated converter with no energy storage. The grid asset is used as the bulk energy storage element at the fundamental frequency. The converter reflects the asset value on the grid and can do so within a sub-cycle of

the fundamental frequency. The converter has a fail-normal mode of operation and therefore does not degrade system reliability. In addition to providing dynamic control, it is desirable to enhance the control capabilities of the asset. This is realized through the implementation of the principle of virtual quadrature sources. Details on the novel concepts, applications, and implementation methods are researched as part of this dissertation.

1.3 OUTLINE OF CHAPTERS

The dissertation is divided into ten chapters. A detailed review of prior art is presented in Chapter 2. This chapter lists existing solutions, both static and dynamic, that are currently used in power networks.

The basic concept of thin AC converters, (TACCs) is introduced in Chapter 3. The proposed concept is presented and illustrated using applications where the ability to use existing grid resources for dynamic control is demonstrated.

The principle of virtual quadrature sources is presented in Chapter 4. Providing enhanced control capabilities, such as phase angle and, or harmonic compensation with no bulk energy storage, in a single-phase system is discussed. The concept is formulated analytically and verified through simulations and experiment. Applications of the concept of VQS are discussed in Chapter 5. This chapter considers each application and details the operation and control methods both through simulations and experimentally.

Chapter 6 focuses on scaling of the direct-AC converter or TACC. A multilevel converter topology is proposed to enable scaling to realistic voltage and power levels. The modes of operation and control of the converter are presented. Challenges with commutation and snubbers are discussed and methods to implement the cascaded converter are presented. Fault modes of the converter have been studied in Chapter 9. A specific topology is used to understand possible fault modes and the repercussions of different fault types.

The ILSTATCOM is the focus of Chapters 7, 8, and 10. These chapters consider a specific application of the proposed concepts and illustrate the basic

principle of operation, operation of multiple ILSTATCOM's at a system level, and actual design and implantation of the concept in a medium voltage prototype.

CHAPTER 2

ORIGIN AND HISTORY OF PROBLEM

2.1 INTRODUCTION

Growth in the consumption of electrical power and a growing increase in the penetration of renewable resources are stressing the existing power grid. The power system as it stands today is not equipped to handle the steady growth in consumption of power and dynamically changing conditions.

The growing importance of the sustainability of the power grid and the constantly increasing consumption of electric power has resulted in more serious attention towards renewable energy sources such as wind and solar power. This increased awareness is also causing more stringent requirements on the operation and control of the power sector. The two main factors that dictate the mode of operation of the power system are reliability and controllability, as the power utilities today need to supply power reliably at a low cost and energy efficiently using environmentally friendly forms of energy [1].

The power system is divided into three sectors, generation, transmission, and distribution. The system interconnects the points of generation to the points of consumption through the transmission and distribution networks.

The power grid today is controlled using static resources. These resources or assets are switched in and out of the grid on long time scales typically based on forecasting and predetermined operating points. So far this method of control with the existing resources has proved to be adequate for the safe and reliable operation of the grid. With the complex and dynamically changing characteristics of renewable resources and changing loads that we see today, there is a growing need for dynamic control of the grid to ensure safe and reliable operation [2].

In addition to the resources available on the grid, controllability is affected by the structure of the system. Distribution power networks in the U.S. are mostly radial in structure. This grid structure has been adopted primarily because of the

ease with which it can be controlled. The reliability of these networks, however, is fairly poor compared to meshed or networked systems. Utilities today are transitioning to meshed systems for increased reliability. The drawback with meshed systems, however, is the lack of controllability.

Meeting these increasing requirements on the power grid is a challenging task. Solutions to providing enhanced dynamic control capabilities on the grid have been proposed [3], [4] and will be presented in this chapter. Some examples of existing grid resources, or static resources, will also be discussed.

2.2. STATIC AND DYNAMIC GRID CONTROL

Static grid control is control of the power grid in steady-state. The power system at the consumer end can be characterized by constantly changing loads. Supplying power to these loads involves the movement of power from the points of generation to the points of consumption. Statistical tools such as load forecasting are typically used to predict the operating point of the system for specific loading levels, while accounting for factors such as changes in season and time of day. These tools are used by network operators to determine the control effort necessary to facilitate safe and reliable operation of the grid while ensuring the required power throughput.

Examples of devices on the grid that can be used in the steady-state control of the power system include mechanically switched capacitors [5], [6] and load tap changers [7], [8]. These devices work well when the system operating point needs to change within a few cycles (or longer) of the fundamental frequency, i.e. the system operating point is moved from one state to another within a relatively long time period. The major problem with mechanically operated static resources is the wear and tear of the components. The slow response time is inherent to these devices and operation is therefore limited to slower control loops in the system. Commercially available mechanically switched capacitors have a response time of about 100 ms. This would mean that the device would take about six cycles of the fundamental frequency to respond.

While some portion of grid operation can be predicted using statistical tools, a significant part is dynamically varying and cannot be predetermined or predicted. Penetration of renewable energy sources such as wind power changes the nature of the power grid because of the dynamics, complex fault modes, and possible loss in generation. The resulting network is characterized by unpredictable generation and load patterns, and complex operating conditions. It is therefore necessary to use controllable elements on the grid that will allow the system to dynamically adapt to changing conditions and alleviate issues associated with grid dynamics.

Power utilities today operate with large safety margins to ensure grid stability when faults occur in the system. Generation reserves and operation of transmission lines with conservative safety margins are some methods used today.

In the early 1980s flexible AC transmission systems (FACTS) were proposed as a means to control the AC transmission, sub-transmission system, and distribution networks [9], [10], [11]. FACTS devices use semiconductor switches with passive elements and, or energy storage to dynamically control parameters in the network. Some advantages of this technology include a sub-cycle response time and flexible control capabilities with minimal losses compared to mechanically switched devices.

2.3 STATIC RESOURCES ON THE POWER GRID

Stable, reliable, and effective operation of the power grid requires control of two parameters. The first is the bus voltage at every node in the system and the second is the flow of current through the lines. By way of an example, Figure 2.1 illustrates a simple two bus system. Bus 1 and 2 are connected by a line with finite resistance and reactance. The flow of power in line 1 is governed by the difference between the phasor voltages at the two ends of the line and the reactance of the line.

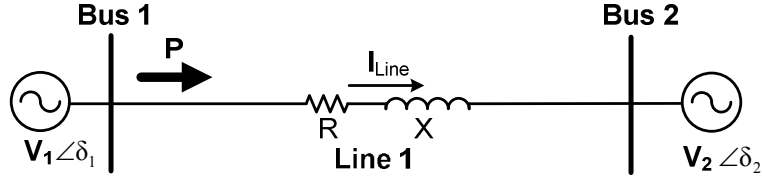


Figure 2.1: Two-bus system

$$\begin{aligned}
 P &= \text{Real Power} = \frac{V_1 V_2}{X} \sin \delta \\
 &= \frac{V^2}{X} \sin \delta
 \end{aligned} \tag{2.1}$$

$$\begin{aligned}
 Q &= \text{Reactive Power} = \frac{V_1 V_2}{X_s} \cos \delta - \frac{V_2^2}{X_s} \\
 &= \frac{V^2}{X_s} (\cos \delta - 1)
 \end{aligned} \tag{2.2}$$

Here, it is assumed that $|V_1| = |V_2| = |V|$, $V_1 \angle \delta_1$ is the voltage at bus 1, $V_2 \angle \delta_2$ is the voltage at bus 2, $\delta = \delta_1 - \delta_2$ i.e. difference between the angles at the sending and receiving ends, V is the magnitude of the bus voltage, and X is the reactance of the line.

The above equations have been formulated assuming the line impedance is purely reactive, in this case inductive. Series resistance of the line has been neglected. The current in the line can be controlled by varying either the impedance of the line or the phase angle difference between the voltages at bus 1 and bus 2. Devices that are used to control the current and thereby power flow in the line control one of the two parameters mentioned above, i.e. X and, or δ . As an example, the phase shifting transformer (PST) controls power flow in the line by controlling the angle δ .

Control of the voltages at every node in the system can be achieved using one of two methods. The first, a direct method of control uses voltage regulators to control the direct component of the voltage. The second method is an indirect method where voltage control is achieved by controlling reactive power. Bus voltage magnitudes in the power system are typically controlled to lie within a

$\pm 5\%$ droop. Examples of devices that provide control of voltage magnitudes include mechanically switched capacitors (MSCs) and load tap changers (LTCs).

The following sections will focus on different types of devices that are typically used in power system networks to provide control of voltage magnitudes and phase angles. Principle of operation, advantages and limitations of each technology will be presented.

2.3.1 MECHANICALLY SWITCHED CAPACITORS (MSC)

The mechanically switched capacitor (MSC) is a low cost device that is used to stabilize the voltage in a power network. The MSC provides leading reactive VARs to control the voltage. MSCs are commercially available through companies like General Electric (GE), ABB, and Siemens.

These capacitors are available in a wide range of voltages from 4.1 kV to 765 kV [5] at hundreds of MVARs. Figure 2.2 illustrates a MSC from ABB [12]. This specific product is a pole mounted capacitor.



Figure 2.2: Pole mounted capacitors for voltage control in distribution networks, [5]

Most if not all commercially available mechanically switched capacitors are available for either fixed or variable applications. The schematic shown in Figure 2.3 details the various components of an MSC.

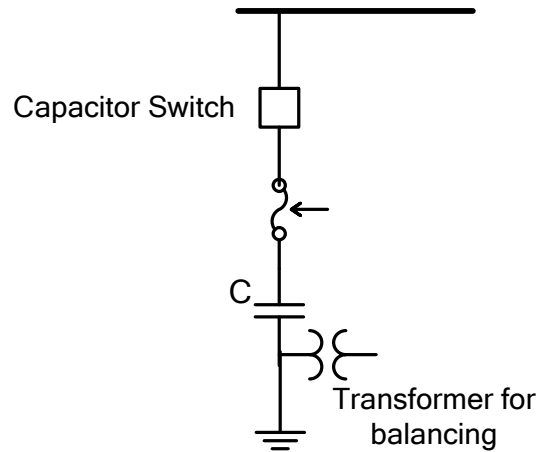


Figure 2.3: Schematic for a mechanically switched capacitor (MSC)

The capacitor is either switched in or out of the network using either a vacuum switch or an SF6 breaker. Typical response times for these switches are 100 ms and 120 ms respectively. With the MSC connected to the grid the capacitance on the grid increases by a value of C . The capacitance cannot be dynamically varied; it has fixed value of C . The MSC provides the ability to control grid voltage and is most effective under steady state conditions. The MSC can also operate based on local measurements. The limiting factor however is the response time of the device.

The MSC provides inadequate reactive power support during voltage dips on the grid. The reactive power generated by the MSC is proportional to the square of the line voltage. Therefore under low voltage conditions, the MSC provide insufficient voltage support. Also, these devices are typically used with reactors and damping circuits to prevent resonances on the system. This adds to both cost and complexity of the device.

2.3.2 LOAD TAP CHANGERS (LTC)

The load tap changer is a device used to control the voltage magnitude in a distribution network [13]. The voltage of the distribution transformer winding is increased or decreased in discrete steps using a tap changer. An increase in the voltage is referred to as positive tapping and a decrease in the voltage is called negative tapping. Load tap changers can be classified as off-line tap changers

and on-load tap changers (OLTC) [14]. Tap changers are located on the windings of the transformer. Typically off-line tap changers are used on the low voltage winding of the transformer, while the OLTC is located on the high voltage (low current) winding. Off-line tap changers are used where an interruption in the supply of power can be tolerated. This is because the transformer needs to be de-energized to change the tap setting either manually or using switches. For OLTC's the tap setting of the transformer is changed while the transformer is energized. During the transition from one tap setting to the next there is a short period of time when both the taps are shorted. This results in large currents that are controlled using impedance. Locating the OLTC on the high voltage winding of the transformer will minimize the level of nominal as well as short circuit current. This is the primary reason that OLTCs are located on the high voltage winding.

There are three types of tap changers that are available, mechanical, thyristor assisted, and solid state. In the mechanical tap changer the tap settings are changed using a tap selector and diverter switch. The tap selector is used to make a change from the initial to the final tap position. The diverter switch is used to prevent shorting between two tap settings by providing a path through impedance. Commercially available OLTCs from ABB use a resistor as the impedance [15]. Figure 2.4 illustrates a commercially available mechanical OLTC.

Mechanical tap changers are sluggish devices and require regular maintenance because of wear and tear. This is both labor and cost intensive. Additionally, the efficiency of the device is poor because of the losses in the resistor during tap transitions.



Figure 2.4: On-load tap changer (OLTC), [15]

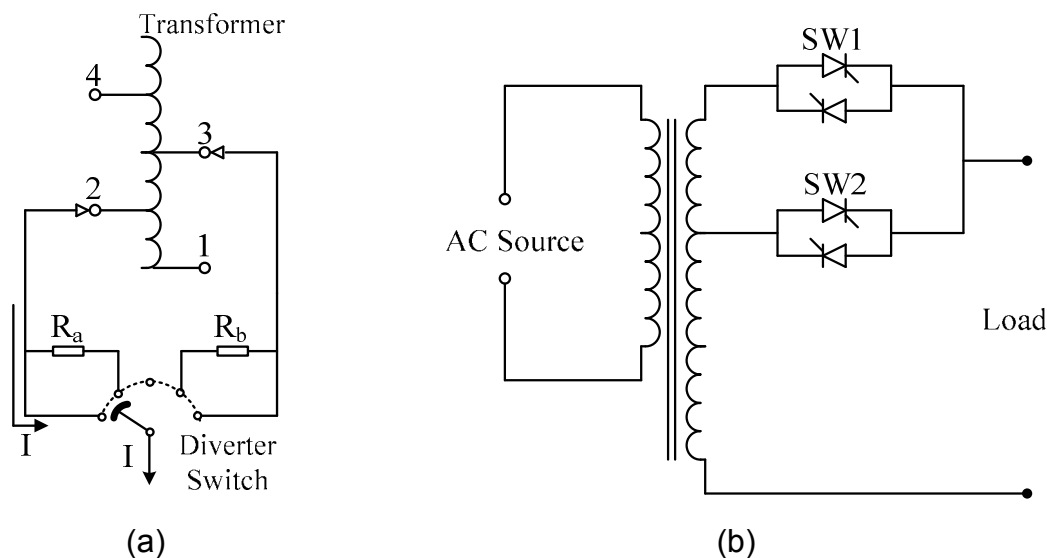


Figure 2.5: On-load tap changer, (a) mechanical, (b) solid-state

The thyristor assisted tap changer [16] uses a thyristor to provide a path for the current during the tap transitions. This device requires less maintenance compared to the mechanical OLTC. Losses in the thyristor-assisted OLTC are significant because of the conduction losses of the thyristor during normal operation.

The solid-state OLTC uses thyristors for both the selector as well as diverter switches [17]. There is an increase in the cost and complexity because of the use of semiconductors. Figure 2.5(a) and (b) illustrate the mechanical and solid-state OLTC's.

The OLTC is a sluggish device with a response time of a couple of cycles at the fundamental frequency. The mechanical OLTC shown in Figure 2.4 has a typical response time of 50 ms, i.e. it takes 50 ms to change from one tap position to another. This is roughly three cycles of the fundamental frequency. Similar to MSCs, OLTCs are operated either with localized or centralized control. In either case the OLTC cannot provide any kind of dynamic support on the power grid.

2.3.3 PHASE SHIFTING TRANSFORMERS (PST)

The phase shifting transformer (PST) [18], [19] is a device used in the power system to control the flow of real power. PSTs operate by injecting a voltage (V_q) in quadrature with the line voltage (V_a). The phasor sum of the line voltage and injected series voltage is an output voltage (V_a') with controllable phase. The schematic shown in Figure 2.6(a) illustrates the principle of operation. The amount of phase-shift that can be realized using the PST is dependant on the magnitude of the injected quadrature voltage. This value impacts the size and rating of the device.

The phasor diagram for a PST with a single active part that provides positive phase-shift control is shown in Figure 2.6(b). This type of PST is called an asymmetrical PST because of the unidirectional control range (in this case positive angle). 3-phase implementation of the PST is shown in Figure 2.6(c).

PST's are similar to LTCs with respect to efficiency, cost, and response time. Thyristor based PSTs are also commercially available but are limited in use because of issues with short circuit protection [20].

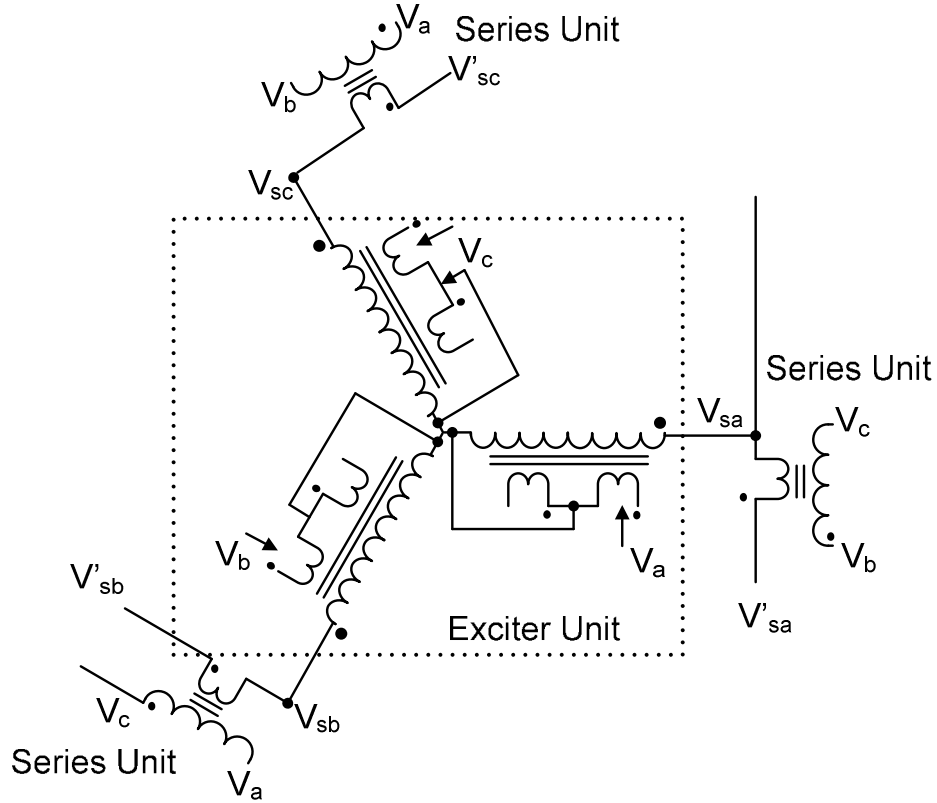
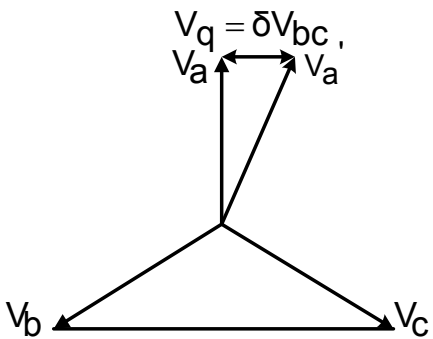


Figure 2.6: (a) Schematic for a phase shifting transformer, (b) phasor diagram, (c) three-phase implementation of the PST

The effect of a PST in a simple two line, two-bus system is shown in Figure 2.7. The phase angle of the voltage is changed by V_{PST} , this results in an

increase in the current by ΔI_1 . The change of power flow in line 1 causes a change in line 2. The simple system used in this example illustrates the basic principle. The impact of PST's in a large system is not captured in this example.

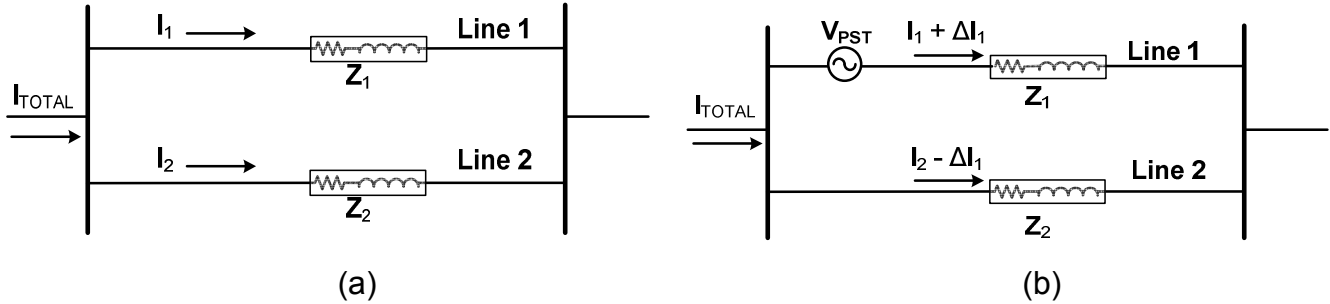


Figure 2.7: Two lines, two bus system: (a) without PST, (b) with PST

The PST can be controlled either with local measurements or centralized (dispatch) control [21]. In dispatch mode the operating point of the PST is predetermined using load flow analysis and load forecasting. The set-points are then dispatched to the device.

The PST is an expensive and sluggish device with no dynamic control capabilities [22]. The PST also has complex fault modes because of the cross-coupling between phases, i.e. the effect of a fault on any one phase will affect the other phases. PSTs are typically custom made for utilities by companies like ABB because of the small volumes and high cost of these devices.

2.4 DYNAMIC GRID CONTROL

Dynamic control on the power system is needed during unforeseen changes on the grid that require control in a sub-cycle time frame [23]. This type of control is necessary to maintain uninterrupted supply of power during conditions such as faults.

Dynamic control on the power grid is essential to achieve the following:

- Control of the flow of power along selected routes to ensure minimal loop flow, i.e. dealing with unforeseen changes in routing of power because of distributed resources (renewables).

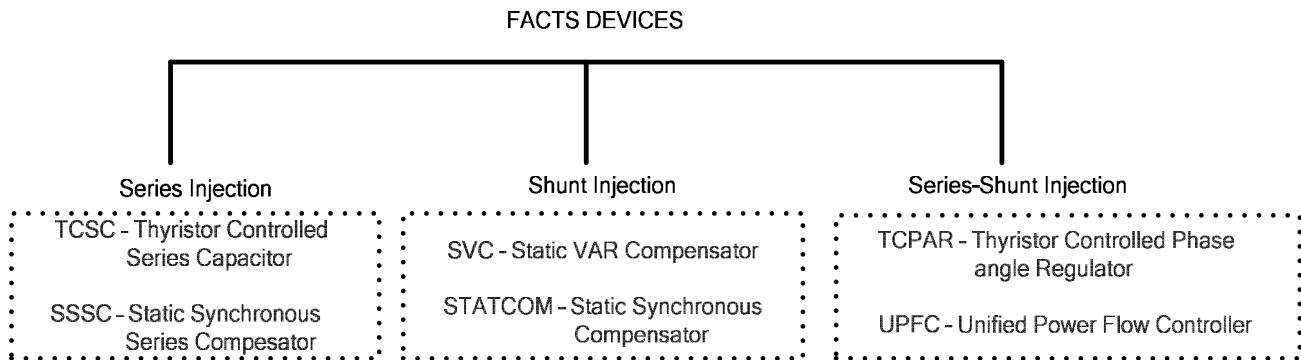
- Better utilization of the existing infrastructure, i.e. increased loading of transmission lines while operating within secure limits
- Increase the power throughput of the network
- Damp power system oscillations
- Help the system ride through faults

To achieve the above control capabilities on the network devices that provide dynamic control capabilities are required. Current approaches to achieving the above mentioned control capabilities include flexible AC transmission system (FACTS) devices. FACTS devices will be discussed in detail in the following section. Operating principles and the control capability of each device will be presented.

2.4.1 FACTS SOLUTIONS TO GRID CONTROL

FACTS devices provide control of the AC parameters in a network [24], [25]. These devices can be classified based on the mode of connection to the grid, as shown in Table 2.1. The first set of FACTS devices discussed are series connected FACTS devices.

Table 2.1: Classification of FACTS devices



2.4.1.1 SERIES FACTS DEVICES

Series FACTS devices provide control of the power flow in transmission lines. As explained earlier, this can be achieved by either varying the reactance

of the line or by controlling the phase angle δ . The flow of real power in a line is give by equation (2.3).

$$P = \frac{V_1 V_2}{X} \sin \delta \quad (2.3)$$

Here, V_1 and V_2 are the magnitudes of the sending and receiving end voltages respectively, δ is the phase angle of the driving voltage of the line, and X is the reactance of the line.

Series FACTS devices can categorized based on the type of control method, i.e. control of reactance or control of phase angle. To ensure full utilization of the transmission lines on the network the power throughput of the network needs to be increased. Power throughput in any network is limited by the line that reaches its thermal capacity first. This could lead to under utilization of a significant portion of the system. Therefore, series compensation devices are used to increase utilization of the network.

Transmission lines are primarily inductive. To increase the power throughput of the network the inductive reactance of the lines operating close to its thermal limits needs to be increased, and that of the under-loaded lines needs to be decreased. This can be done by connecting capacitors and, or inductors in series with the line [26]. Typically series compensators are used to decrease line reactance, i.e. capacitors are connected in series with the line. A simplified equivalent circuit for a two bus power system is shown in Figure 2.8.

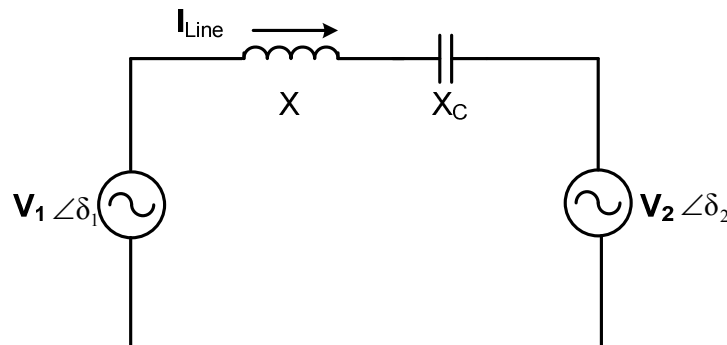


Figure 2.8: Two-bus system with series capacitor

The effective line impedance with the capacitor is given by equation (2.4).

$$X_{eff} = X - X_C$$

$$X_{eff} = (1 - k) X$$

$$k = \frac{X_C}{X}, \text{ and } 0 \leq k < 1 \quad (2.4)$$

Where, X_{eff} is the effective impedance of the line, X is the line impedance, X_C is the reactance of the compensator, and k is the degree of compensation.

The degree of compensation k is defined as the ratio of the injected capacitive reactance to the inductive reactance of the line. The degree of compensation typically used with series compensation devices is 25% to 75%.

The simplest topology for a series compensator is the thyristor switched series capacitor (TSSC) [27]. The TSSC is a device with a capacitor connected in parallel to a bypass (thyristors connected in anti-parallel), as shown in Figure 2.9.

The TSSC is simple in method of operation. It has two modes, an ON and an OFF mode. When the valve is ON, the effective capacitance injected in the system is zero. With the valve OFF, the capacitance injected in the system is equal to C . The TSSC is implemented by series connecting multiple devices to realize discrete step changes in capacitance.

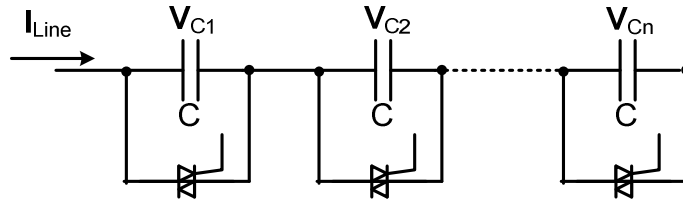


Figure 2.9: Thyristor switched series capacitor

The amount of series capacitance injected in the line can be increased by connecting a reactor in series with the thyristor valve. The resulting topology is known as the thyristor controlled series capacitor (TCSC) [28], [29].

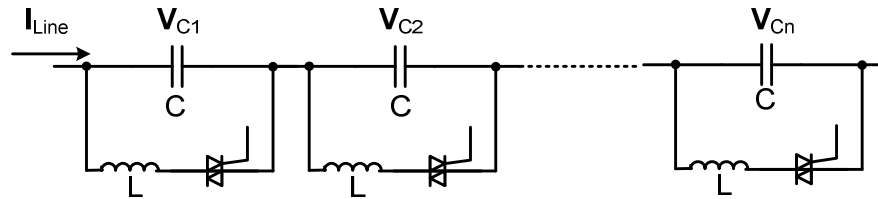


Figure 2.10: Thyristor controlled series compensator

The TCSC has a much wider range of control compared to the TSSC. The TCSC has four modes of operation. The first mode is with the valve open (blocking mode), where the capacitance injected by the TCSC is C . The second mode of operation is with the valve conducting (by-pass mode). In this mode the effective reactance injected by the device is inductive. This mode is typically used under faulted conditions when the capacitance of the line needs to be minimized. The third and most important mode is the capacitive boost mode. This mode allows the effective capacitance to be increased to about three times the actual value of the capacitor. This is achieved by controlling the valve to trigger right before the zero-crossings of the line current. The resulting circulating current adds to the line current through the capacitor causing an increased voltage across C .

$$X_{TCSC}(\alpha) = \frac{X_C X_L(\alpha)}{X_L(\alpha) - X_C}$$

$$X_L(\alpha) = X_L \frac{\pi}{\pi - 2\alpha - \sin(2\alpha)} \quad (2.5)$$

Where, X_{TCSC} is the effective impedance of the TCSC. This impedance of the TCSC comprises of a fixed capacitive reactance X_C and a variable inductive reactance, X_L which is a function of the delay angle α .

The final mode is the inductive boost mode. This mode does the opposite of the previous mode and is highly undesirable, as it increases the effective inductance of the line.

Series capacitive compensation has significant drawbacks. As the device is connected in series with the line it needs to be designed to handle high fault currents or it needs to be by-passed during a fault. By-passing the device under faulted conditions is undesirable from a system perspective as this decreases the stability margin of the system. Complex methods have been proposed to control the series compensation device to achieve both an increase in the stability margin as well as limit the exposure of the device to faulted conditions.

Another problem with series capacitors is the possibility of sub-synchronous resonance occurring in the system. This is a phenomenon that occurs at a

frequency below the operating frequency of the system because of the interactions between of the mechanical frequency of the turbine-generator shaft and the electrical resonant frequency of the series LC circuit (formed by the transmission line). The phenomenon can result in severe damage of the generator shaft.

Connecting a capacitor in series with the line is equivalent to connecting a voltage source that lags the current by 90° in series with the line. The static synchronous series compensator (SSSC) is a device inserted in series with the transmission line that can generate a voltage source of arbitrary angle, i.e. it can emulate a series connected reactance [30].

The SSSC is a converter based FACTS device that has a coupling transformer, a solid-state voltage source converter, and a capacitor, as shown in Figure 2.11(a). The SSSC can be controlled to inject a voltage of any magnitude and phase in series with the transmission line. This device is typically controlled to inject a voltage that leads or lags the current by 90° .

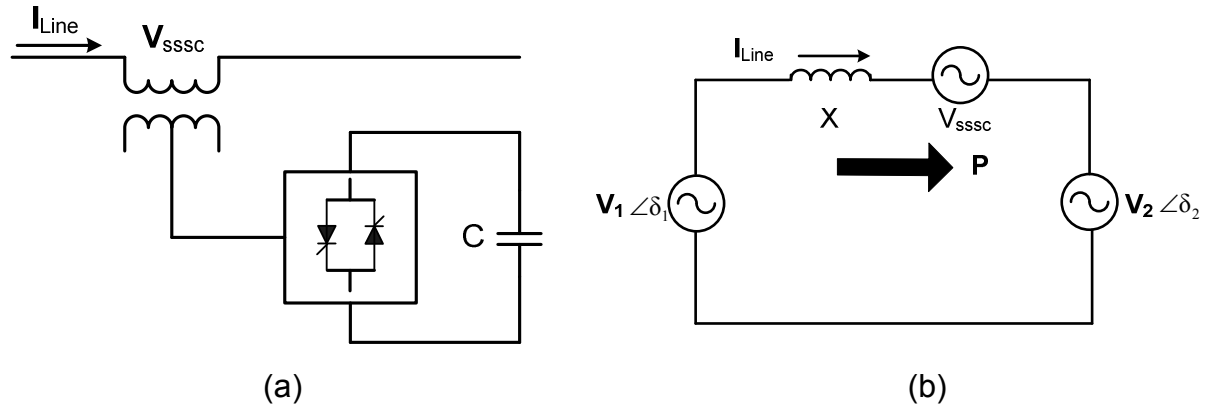


Figure 2.11: Static synchronous series compensator

The SSSC shown in Figure 2.11(a) can be modeled as an equivalent voltage source as shown in Figure 2.11(b). As the SSSC is a full converter based device there is a wide range of flexibility in the control range.

The effect of the SSSC on the real power in the system is given by equation (2.6).

$$P = \frac{V^2}{X_L} \sin \delta + \frac{V}{X_L} V_{SSSC} \cos \frac{\delta}{2} \quad (2.6)$$

Where, $\delta = \delta_1 - \delta_2$ i.e. the difference between the angles of the sending and receiving end voltages, V is the magnitude of the sending and receiving end voltages, X_L is the reactance of the line, and V_{SSSC} is the voltage injected by the SSSC.

The sign of V_q would reflect the nature of compensation, i.e. capacitive or inductive. A positive V_q indicates a voltage source lagging the current by 90° (capacitive) and a negative V_q would mean inductive compensation, where the voltage leads the current by 90° .

A significant advantage of the SSSC versus a capacitor-based compensator is the ability to generate a voltage source independent of the line current. This is desirable as it limits the possibility of resonances occurring in the system. Additionally, the SSSC has been shown to be more effective in increasing the transmitted power over $0 \leq \delta < 90^\circ$ compared to the TCSC [31]. This is quite an important advantage of the SSSC over the TCSC as it provides greater improvement for the given angle range.

Drawbacks of the SSSC include high cost and complexity because of the full converter, coupling transformer, and DC energy storage capacitor.

2.4.1.2 SHUNT FACTS DEVICES

Shunt compensators are devices typically used to provide voltage stability in the power system. Voltage control in a power network can be achieved by connecting a voltage source in shunt to generate or absorb reactive power.

Consider the simple two-bus system used in Figure 2.12. The voltage at each end of the line is assumed to be of equal magnitude, i.e.

$$|V_1| = |V_2| = |V| \quad (2.7)$$

Here, V_1 is the sending end voltage, V_2 is the receiving end voltage, and V is the magnitude of the sending and receiving end voltage.

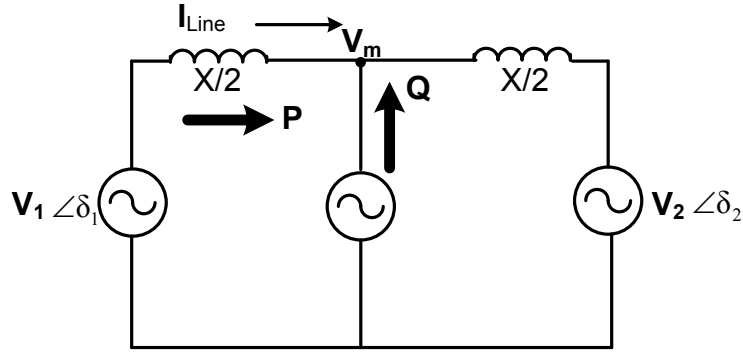


Figure 2.12: Two-bus system with compensation

Dividing the line into equal segments gives the line a voltage profile with a minimum at the mid point. To control the voltage at the mid point of the line an ideal reactive power compensator is used, shown in Figure 2.12. The voltage at the mid point of the line (V_m) can be controlled to be equal in magnitude to V_1 and V_2 . Figure 2.13 illustrates the phasor diagram for the given network parameters.

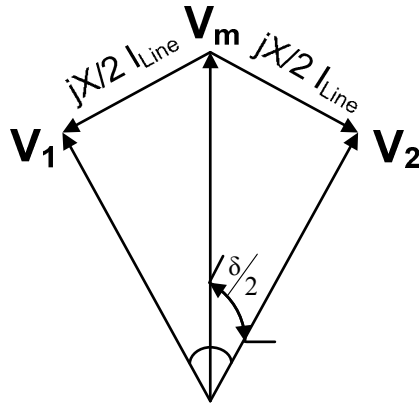


Figure 2.13: Phasor diagram for midpoint shunt compensation

Adding a shunt compensator at the midpoint of the line provides voltage support at the mid point and results in an increase in the amount of real power that can be transmitted through the line, i.e. the real power transfer can be doubled, as shown by Equation (2.8). To increase transfer of real power, the shunt compensator needs to be capable of generating a significant amount of reactive power. For this example the reactive power requirement is four times

the initial value, this makes the shunt compensator undesirable for control of real power.

$$P = \frac{2V^2}{X} \sin \frac{\delta}{2} \quad (2.8)$$

$$Q = \frac{4V^2}{X} \left[1 - \cos \frac{\delta}{2} \right] \quad (2.9)$$

Here, V is the magnitude of the sending and receiving end voltages, $\delta = \delta_1 - \delta_2$ i.e. difference between the angles at the sending and receiving ends, and X = line reactance.

Shunt compensators are however suitable for providing voltage stability on the grid as the voltage at the load centers can be effectively controlled using these devices. Under lightly loaded conditions, inductive compensators can be used to prevent overvoltages, while capacitive shunt compensators can be used to provide voltage support when the system is heavily loaded.

Shunt compensators can be categorized as variable impedance type and switching type compensators [32]. Examples of variable impedance type compensators are shown in Figure 2.14(a) to (d).

The variable impedance type shunt compensators are essentially passive elements connected in series with bidirectional switches.

The thyristor controlled reactor (TCR) shown in Figure 2.14(a) is an inductor with a bidirectional switch [33]. When reactive VARs need to be absorbed the TCR is switched into the system. The TCR is controlled by controlling the firing angle of the thyristors. The effective admittance and current of the TCR are given by equation (2.10) and (2.11) respectively.

$$I_L(\alpha) = \frac{V}{\omega L} \left[1 - \frac{2}{\pi} - \frac{2}{\pi} \sin 2\alpha \right] \quad (2.10)$$

$$B_L(\alpha) = \frac{1}{\omega L} \left[1 - \frac{2}{\pi} - \frac{2}{\pi} \sin 2\alpha \right] \quad (2.11)$$

Here, V is the voltage across the TCR, ω is the frequency in radians, α is the firing angle, I_L is the current through the TCR, and B_L is the effective admittance of the TCR.

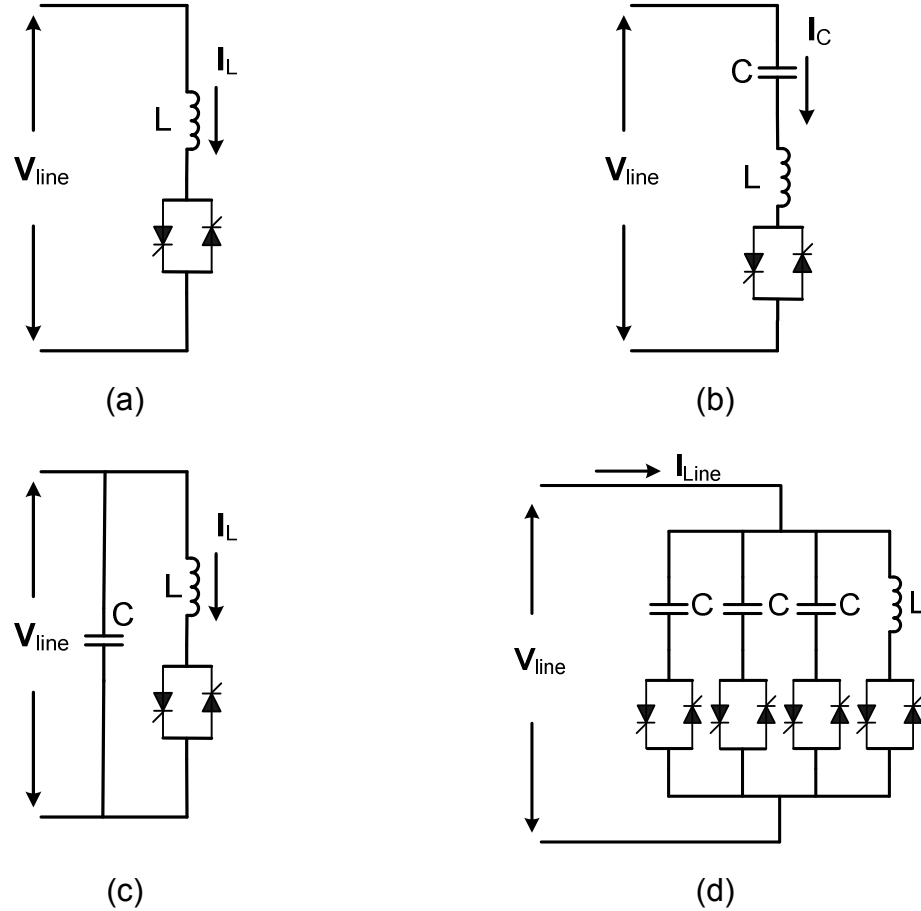


Figure 2.14: Variable impedance shunt VAR compensators: (a) TCR, (b) TSC, (c) FC-TCR, (d) TSC-TCR

The inductance of the TCR can be varied from 0 to a maximum value by controlling the firing angle. The main drawback of the TCR is the non-sinusoidal, harmonic rich current generated by the device. The high harmonic content of the current is undesirable and can cause further distortion of the grid parameters. To reduce the effects of these harmonics LC and LCR filters are used that are tuned to filter the dominant harmonics.

The thyristor switched capacitor (TSC) shown in Figure 2.14(b) is a device used to generate leading VARs for voltage control on the grid [34]. The device has a capacitor connected in series with a bidirectional valve and a surge current limiting inductor. The TSC is similar to an MSC, i.e., it can be switched in or out of the grid and provides a fixed value of capacitance. To connect the capacitor to

the grid at any instant of time the voltage across the capacitor needs to be equal to the line voltage, i.e., the two voltages need to be matched. If the capacitor is switched in with a voltage mismatch, a large surge current is generated that can cause an undesirable transient at the node. This requirement defines the limit for the response time of the device. In real systems the TSC has a response time of up to one cycle of the fundamental frequency.

Controllable leading and lagging VARs can be achieved by combining a fixed capacitor (FC) and TCR. The FC-TCR VAR compensator is shown in Figure 2.14(c) [35]. The FC generates a fixed amount of leading VARs to support the grid. The FC can also be used as a shunt path for the dominant harmonics generated by the TCR.

The VARs generated by the FC-TCR can be controlled by controlling the firing angle of the TCR. As the firing angle of the TCR is varied the inductance (lagging VARs) is controlled. The total reactive VARs generated by the device is given by,

$$Q = Q_L - Q_C \quad (2.12)$$

Where, Q_L is the inductive VARs generated by the TCR, and Q_C is the leading VARs generated by the FC.

Figure 2.15 shows the variable VARs generated by the FC-TCR. The demand versus output characteristic is shown, where the total reactive VARs generated by the FC-TCR is given by Equation 2.12.

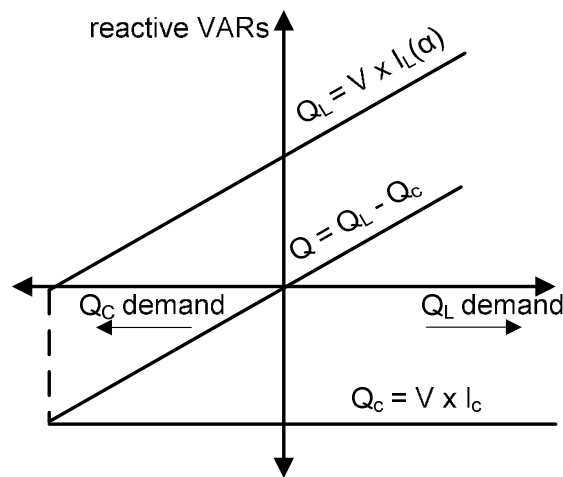


Figure 2.15: Control range for FC-TCR

To realize fully controllable capacitive VARs a combination of the TSC and TCR is used. Figure 2.14(d) illustrates one such example, where three TSCs are connected in parallel with a TCR. Each TSC provides a fixed number of VARs that can be absorbed if in excess by controlling the TSR. Discrete steps in leading VARs can be obtained by switching in additional TSCs while controlling the firing angle of the TCR to absorb the excess VARs at every stage.

Shunt VAR compensators (SVC) are a relatively low-cost solution to voltage control on the grid. These compensators are limited in functionality under reduced line voltage conditions, as in the case of MSCs and SVCs. SVCs have a better response time compared to MSCs, but are still quite sluggish compared to switching converter-based compensators.

The second type of reactive compensator is the switching converter-based VAR compensator [35]. In this case, as in the case of the converter-based series compensator a switching converter is used to generate leading or lagging VARs. The schematic shown in Figure 2.16(a) illustrates a switching converter-based VAR compensator. The control range of the device is illustrated in Figure 2.16(b). The control range of the STATCOM illustrates a 'droop' characteristic, where the terminal voltage is varied proportionally to the VAR regulating current, i.e., the STATCOM is not an ideal voltage compensator. The deviation from the reference voltage (ΔV_{Cmax} , ΔV_{Lmax}), as shown in Figure 2.6(b) determines the slope of the droop.

The static synchronous compensator (STATCOM) is an example of a converter-based VAR compensator [36], [37]. The STATCOM consists of a voltage source converter, coupling transformer, and a DC capacitor. In principle the STATCOM can be controlled to emulate a controllable shunt-connected inductor or capacitor. The operation of a STATCOM is similar to a synchronous condenser. In a synchronous condenser the reactive power at the terminals can be varied by varying the excitation voltage. Similarly, in the STATCOM, the reactive power generated or absorbed is varied using a voltage that is synthesized using a full bridge voltage source converter.

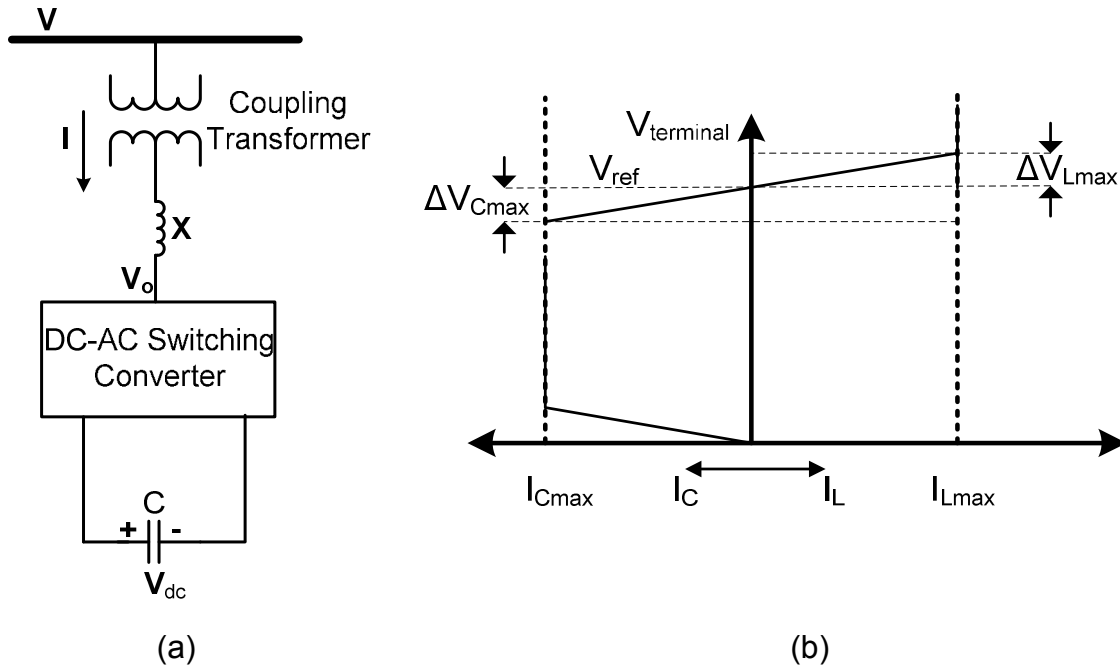


Figure 2.16: Static synchronous compensator (STATCOM), (a) schematic, (b) control range for an ideal STATCOM

The converter synthesizes a voltage in phase with the line voltage which can be varied in magnitude based on the requirements on the grid. With a voltage V_o (voltage at the output of the converter) greater than the line voltage, the STATCOM generates leading reactive VARs. By controlling the voltage to be less than the line voltage, the STATCOM absorbs reactive VARs. Controlling the voltage generated by the STATCOM to be in phase with the line voltage ensures no exchange of real power between the device and the grid.

The STATCOM allows far more flexibility as a shunt compensator compared to the impedance-based devices. The reactive power generated by the STATCOM can be controlled to vary from 100% leading to 100% lagging. The ability to generate reactive power independent of the system operating conditions is a significant advantage of the STATCOM over an impedance-based (SVC) compensator. Problems with the STATCOM arise during faults on the system. The STATCOM is a device that operates assuming three-phase balanced conditions on the grid. Faults on the grid are typically asymmetrical in nature. Under these conditions the STATCOM is unable to synthesize the necessary

VARs to support the grid voltage through the fault. Saturation of the coupling transformer under asymmetrical faults on the system is another issue with the STATCOM [38]. The cost associated with the converter as well as the DC link capacitor is significant especially when compared to the cost of an SVC. Finally, reliability of the compensator is impacted by both the number of components and the energy storage device. The dynamic VAR compensator (DVAR) from American Superconductor and Chain-link STATCOM from Areva are examples of commercially available STATCOMs. The DVAR is a three-phase VSC-based STATCOM that is implemented using low voltage power electronic modules, as shown in Figure 2.17(a). A step-up transformer is used to connect the modules to the power grid. The compensator is available in the range of two to hundreds of MVARs at voltages of up to 49 kV. The VAR rating of the device is increased by connecting modules in parallel. The chain-link STATCOM from Areva is a single-phase STATCOM that uses a chain-link structure (as the name indicates). The STATCOM uses an h-bridge as the basic building block. Areva has demonstrated operation up to 150MVAR at 115kV.



(a)



(b)

Figure 2.17: Commercially available STATCOMs, (a) DVAR, (b) chain-link STATCOM

2.4.1.3 SERIES-SHUNT FACTS DEVICES

Series and shunt compensation can be achieved using a converter-based FACTS device. An example of such a device is the unified power flow controller (UPFC) [39] shown in Figure 2.17.

The UPFC is a device that provides simultaneous control of voltage magnitude and power flow. The UPFC has two three-phase power converters, a DC link capacitor, supply transformer, and a series transformer. A voltage V_{UPFC} with variable phase and amplitude is injected in series with the line through the series transformer. Control of real power is achieved by varying the phase angle of this voltage, similar in principle to a PST. The voltage source V_{UPFC} can emulate a reactance by being controlled to lead or lag the current by 90° .

The versatility of the UPFC lies in its ability to control both real and reactive power independently. By way of an example, assume the voltage injected by the series transformer using converter 2 causes a change in the real power flowing in the line. This would result in real power being drawn from or dumped into the DC link capacitor. The task of converter 1 is to control the voltage across the DC link capacitor and source or sink the real power required by converter 2 through the supply transformer. The UPFC therefore has the ability to shuffle real power back and forth. Reactive compensation can be achieved by controlling converter 1 independent of converter 2.

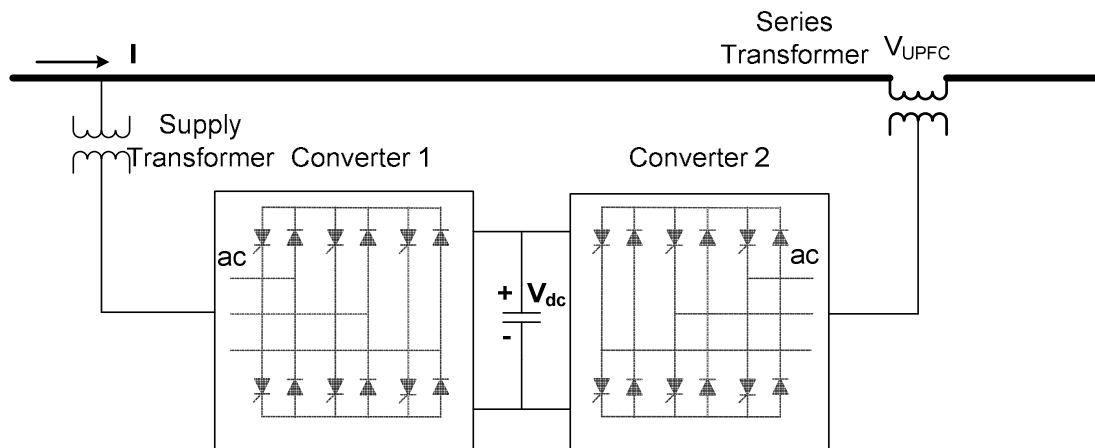


Figure 2.17: Unified power flow controller

The UPFC has a wider range of control than any other device discussed so far. It does however have highest cost and complexity. The power semiconductors, DC link capacitor, coupling, and supply transformers all contribute to the cost of the device.

The first real installation of a UPFC was in 1998. A ± 160 MVA UPFC was installed at American Electric Power's (AEP) Inez substation in Kentucky [40].

An extension of the UPFC is the interline power flow controller (IPFC). The IPFC provides simultaneous shunt and series compensation in a system with multiple lines [41]. The UPFC provides a method to utilize individual transmission lines more effectively. The IPFC on the other hand simultaneously compensates a number of transmission lines at a given substation. Figure 2.18 illustrates an IPFC implemented for three lines. The IPFC is an improved version of the SSSC, i.e., the IPFC essentially comprises of an SSSC per line. The DC link capacitor of all the SSSC's are linked to enable transfer of real power between lines. The advantage of using an IPFC over series impedance-based compensators is the ability to minimize losses in the lines while controlling power flow. The IPFC however has complex control schemes and fault modes because of the common DC link and cross-coupled lines.

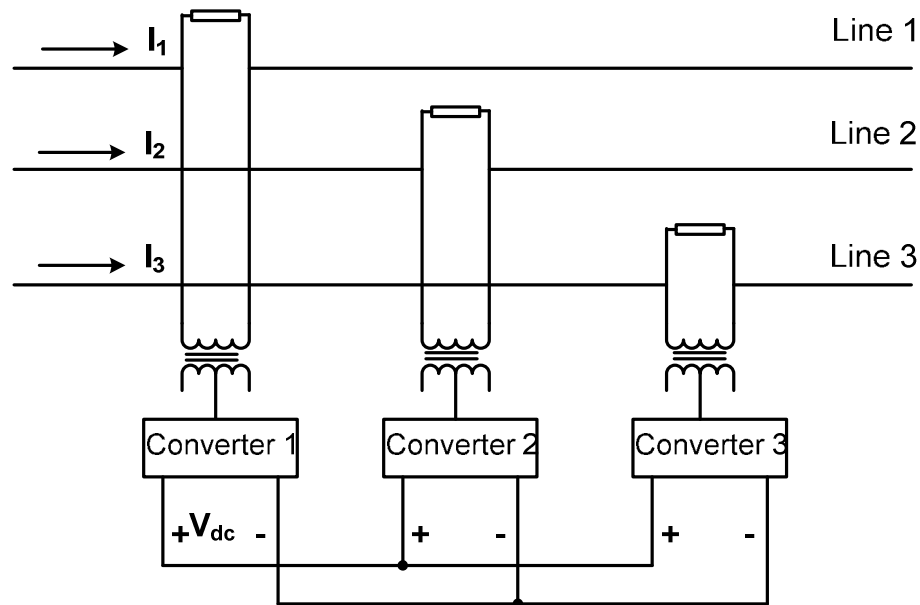


Figure 2.18: Interline power flow controller

2.4.1.4 DISTRIBUTED FACTS (D-FACTS)

The concept of distributed FACTS (D-FACTS) has been proposed in [3]. D-FACTS devices are relatively low-cost compared to conventional FACTS devices

and are smaller and more widely distributed through the networks. Distributing these devices allows widespread control of the system while ensuring high reliability.

The distributed series impedance (DSI) presented in [42] proposes the use of a clamp-on device to provide series compensation, to control real power flow in the line. The schematic shown in Figure 2.19 illustrates the DSI.

The device has a single turn transformer (STT) that is clamped to the line. When no compensation is required, switch S_m is closed. Based on the type of injection required, either switch S_1 , or S_2 is turned on. The electronics required for controlling the device is powered by the transmission line through a current transformer.

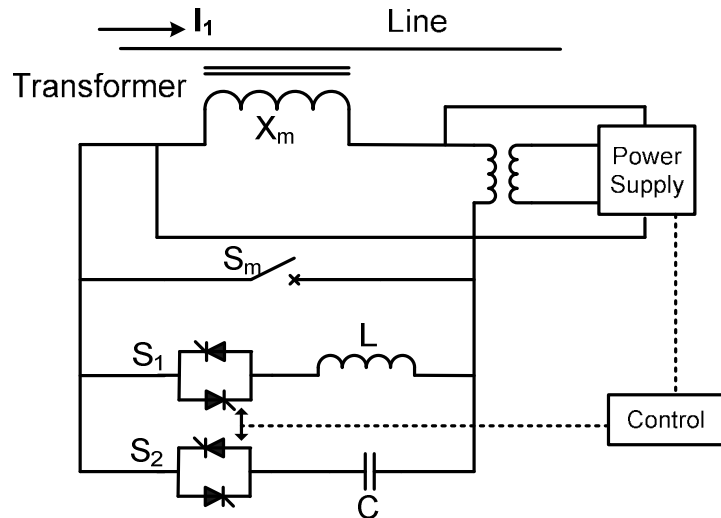


Figure 2.19: Distributive series impedance

The DSI has been demonstrated to provide increased power throughput in the system. This technology seems promising as it is a low-cost solution with minimal components. A simpler version of the DSI, the DSR, has been developed. This device provides only inductive compensation. The device is passive as it has no switches that actively control injection of the reactance. Significant improvement of the transfer capacity of meshed networks has been shown [55].

2.4.2 THE SEN TRANSFORMER

The Sen transformer is a device that can be used to provide simultaneous control of voltage magnitude and phase angle [43]. The transformer comprises an exciter unit and a voltage regulator unit, or impedance regulator unit, shown in Figure 2.20.

Voltage regulation is achieved by using a primary winding in the exciter unit that is excited by the line voltage. This winding is connected in shunt with the line. The secondary of the transformer comprises nine windings (a_1 , a_2 , a_3 , b_1 , b_2 , b_3 , c_1 , c_2 , and c_3), i.e. three windings per-phase. The controlled voltage on the secondary V_{sa} of the transformer is injected in series with the line.

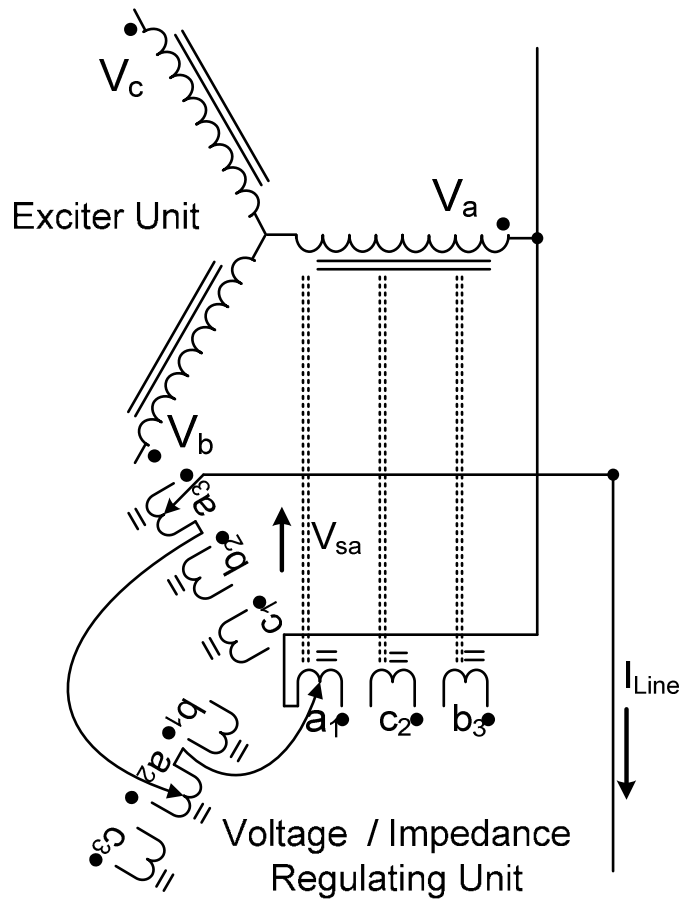


Figure 2.20: Sen transformer

The phasor sum of the line voltage and the selected tap voltage results in the desired output voltage. The schematic shown in Figure 2.20 illustrates the

voltage regulating unit. The same power circuit can be used for the impedance regulating unit. The difference in implementation of the two is in the control. Voltage regulation is achieved by summing the in phase component of the voltage on the secondary winding (with the appropriate tap selection) with the line voltage. Impedance control is obtained by summing the quadrature component (line-to-line voltage) with the phase voltage to realize a voltage that leads or lags the line current by 90° .

The Sen transformer has been shown to have the capability to provide simultaneous control of voltage magnitude and line impedance. It is an expensive and sluggish device because of the high device count, and the number of windings required per-phase to realize the necessary control capabilities. It adds complexity to the power system because of cross-coupling between phases. Simpler schemes of the transformer have been proposed to realize a smaller control range at a reduced cost.

2.5 CONCLUSIONS

There is a growing need for dynamic control in the power system to ensure high reliability and sustainability. The growth in power consumption and the increase in penetration of renewable resources are stressing the grid. Solutions that provide effective utilization of the existing resources are critical in ensuring effective and reliable grid operation.

This chapter presents a survey of existing technologies that provide static and dynamic control of the bus voltages and line currents in the power grid.

The power system today is largely controlled with static resources. These resources are available on the grid as tools that are switched in and out of the system in long time scales. Examples of these resources are mechanically switched capacitors (MSCs) and load tap changers (LTCs). These devices are slow responding and provide control in discrete steps and are thereby unsuitable for dynamic control. Both the MSCs and LTCs can be controlled locally or from a central location (substation). Typical response times for MSCs is about six

cycles of the fundamental, while the LTC can take up to four cycles to provide a step change in control.

Flexible AC transmission system (FACTS) devices provide a solution to dynamic grid control. Series, shunt, and series-shunt FACTS devices have been discussed in detail to illustrate control methods and components required for each device type. Series FACTS devices provide control of the power flow in a line. This is achieved by impedance or series voltage injection using TSSCs, TCSCs, and SSSCs. Shunt compensators are used on the system to provide dynamic voltage control through the control of reactive power. Examples of shunt compensators include static VAR compensators (SVCs), and Static Compensators (STATCOMs).

Finally, devices that provide simultaneous control of voltage magnitude and phase angle have been discussed. The unified power flow controller (UPFC) and Sen transformer are two examples. Both of these solutions are high cost and add complexity to the existing system.

The proposed research aims at providing a method to realize dynamic grid control by utilizing existing grid assets. The concept proposes the augmentation of existing static resources on the grid to realize dynamically controllable smart assets. The solution is low-cost compared to FACTS devices and has high reliability.

CHAPTER 3

THIN AC CONVERTERS

3.1 INTRODUCTION

The objective of the proposed research is to develop a low-cost method for dynamic control of the power grid that utilizes existing grid assets. Current approaches to dynamic grid control aim at using additional black boxes that provide problem centric solutions. Some examples include STATCOMs [36], TCRs [33], and UPFCs [39].

Existing solutions that are relatively lower in cost are also limited in operation, especially faults and fast grid dynamics. These solutions are typically thyristor based. Solutions that are designed to provide enhanced grid support during dynamic conditions, i.e., with sub-cycle response times, are significantly higher in cost and complexity. These are converter-based compensators that use DC-AC converters as a building block. Standard VSC blocks use large energy storage devices in the form of electrolytic capacitors that degrade the reliability of the converter because of the catastrophic failure modes. Finally, issues with scaling of the standard VSC technology has also been a big stop-block in the widespread use of this technology. Because of these issues FACTS devices have seen minimal market penetration. Some commercially available FACTS devices include DVAR (dynamic VAR from American Superconductor) [44], UPFC (installed by American Electric Power) as well as the chain link STATCOM (Areva) [45].

3.1.1 CHARACTERISTICS OF A SOLUTION TO DYNAMIC GRID CONTROL

FACTS solutions are installed on the power grid at points where the device is most beneficial to the system. These devices are added to the system to provide control of voltage and, or power flow. Failure of the devices could result in failure

of sections of the grid that are impacted by the FACTS device. It is therefore important to have a device that is distributed and low-cost to ensure minimal impact of failure of these devices.

The following are characteristics of an ideal solution to dynamic grid control.

3.1.1.1 SINGLE-PHASE IMPLEMENTATION

The power grid is a three- phase system; one therefore assumes the need for a three-phase solution to dynamic grid control. Dynamic control is typically required during contingencies such as faulted conditions and unprecedented changes in load profiles. The majority of these conditions are known to be asymmetrical in nature.

Consider a single-phase asymmetrical fault on the grid. During the fault the voltage on one phase would drop to a value below 0.95. At this point, dynamic VAR support is required to stabilize the voltage and help the system ride through the fault. VAR compensation capacitors cannot provide the required VAR support because of the reduced line voltage, and also because the capacitors cannot respond fast enough. On the other hand, STATCOMs can support the system through the fault. It is however important to mention that STATCOMs are three-phase devices that are designed and sized for balanced three-phase operation. The relative sizing and cost of the device increase significantly if designed for asymmetrical conditions. The STATCOM will therefore not be able to support the asymmetrically faulted system if not specifically designed for it.

The above example is one case in which a single-phase solution to dynamic grid control would be more fitting. There are however cases when a three-phase solution is more economical and a better approach. Applications discussed later chapter will further justify the single-phase implementation.

3.1.1.2 DISTRIBUTED SOLUTION

There are multiple factors that work in favor of a distributed solution. The geographical area that the power grid encompasses and the need for high reliability in the system are two such factors.

Distributing controllable devices would imply requiring a smaller effort per device, which would further imply a smaller rated and lower cost device. This is because the distributed solution would be closer to the point on the grid that requires support. Also, distributing devices ensures higher reliability as failure of a device would not impact a large part of the network.

Consider a device that provides dynamic VARs on the grid. The distance over which reactive power can be transferred is limited by the X/R ratio of the transmission line. This means reactive power cannot be transmitted over large distances. Distributing the device ensures control in pockets of the grid where the dynamic support is necessary for reliable operation.

The same argument would hold for a device that provides control of active power. Distributing the device would mean smaller control efforts required by the devices to obtain the desired result. This further implies a more cost-effective solution that requires only minimal energy storage, if required.

3.1.1.3 INCREMENTAL SOLUTION

Dynamic changes on the grid are incremental in nature. A drop in the voltage usually occurs around the nominal value. At no point during operation of the power system is there a need for control of the voltage between 0 and 1.0 pu. Similarly, the control of phase angle and in turn active power on the grid is incremental in nature. Small changes in phase angles of the node voltages cause a significant movement of active power. It is quite fair to therefore conclude that an effective solution would need to provide only incremental control of the parameters on the grid.

3.1.1.4 UTILIZATION OF EXISTING ASSETS

Finally, providing a cost-effective solution is key to seeing large-scale penetration of any technology. The component that contributes most to the cost of the technology is the energy storage device. Energy storage is a necessity when providing dynamic control of the grid. The challenge therefore lies in the ability to have a low-cost device that provides the desired control.

Leveraging the existing resources on the grid to provide the bulk energy storage is definitely the answer to providing a cost-effective device. There are a large number of static resources on the grid that provide no dynamic control. Some examples of these resources are LTCs and MSCs. It is therefore ideal to work with the existing grid assets to provide the dynamic control required.

Taking into account the above factors an ideal solution to dynamic grid control is proposed. The approach proposes converting existing dumb grid assets into smart and controllable assets using the concept of thin ac converters (TACC). The proposed solution custom fits the problem of dynamic grid control. This concept would allow for significant cost reduction and enhanced system-level reliability. Discussions on the basic concept that drives this technology as well as details on the modes of operation will be presented followed by some examples.

3.2 BASIC CONCEPT OF THIN AC CONVERTERS

The underlying motive is to achieve dynamic grid control while increasing the economic efficiency at the system-level through the utilization of existing utility assets. Desired dynamic control of the asset is realized using a thin ac converter that consists primarily of power semiconductors and high frequency filter elements with minimal energy storage.

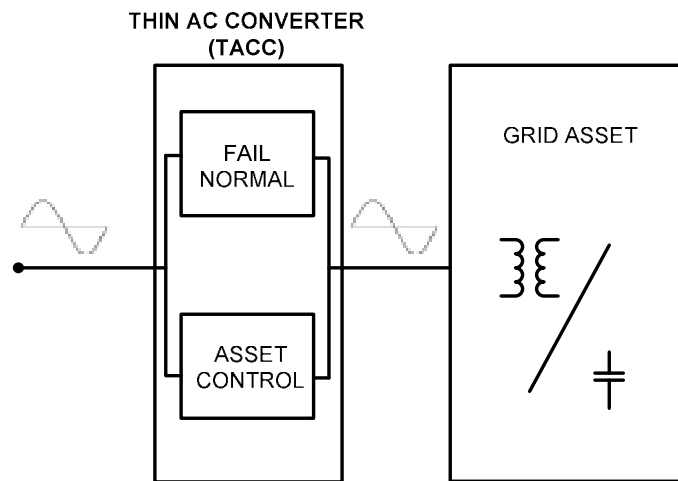


Figure 3.1: Concept of a thin AC converter

The TACC is located between the grid and the asset, as shown in Figure 3.1. This thin converter is a power conditioning interface that reflects the asset value while giving the asset enhanced control capabilities [46]. The characteristics of a TACC are summarized below.

- Dynamic control of assets. This allows the asset to operate under dispatch mode or provide local autonomous control, as needed.
- Direct AC conversion using semiconductor switches, small LC filters, switchgear, and minimal energy storage. This results in a compact converter with a low volume, hence a ‘thin’ ac converter.
- Minimal additional stresses on the asset (e.g., dv/dt , common mode voltages and harmonics), allowing for safe and reliable operation of existing assets even in retrofit applications.
- ‘Fail-normal’ mode of operation. In this mode, failure of the thin converter automatically restores normal function of the asset on the grid.
- Integration with the asset for green-field applications or stand-alone operation in coordination with the asset in retrofit applications.

Figure 3.2 illustrates the basic idea of asset-augmentation and the type of converter used to realize a smart and controllable asset.

Primary concerns that need to be addressed include the size and rating of the TACC with respect to the size of the asset, as well as the cost benefits of the TACC over FACTS devices.

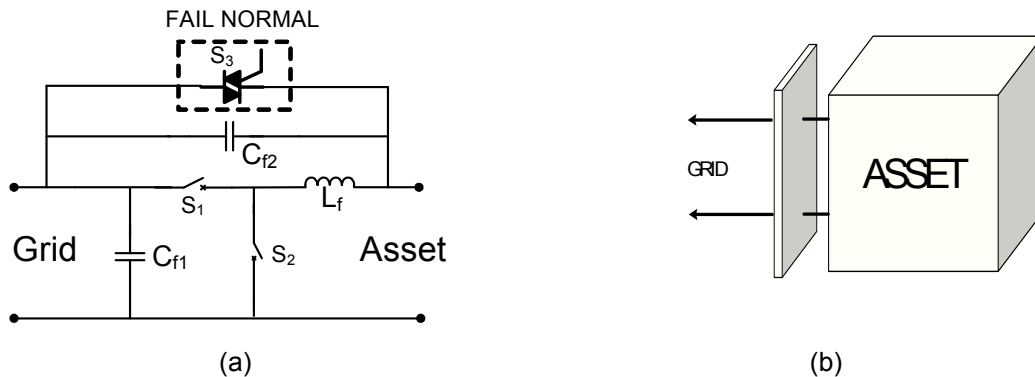


Figure 3.2: Thin AC converter building block

The voltage and power ratings for TACCs vary, depending on whether the device is to be used in distribution, sub-transmission, or transmission applications. Important voltage ranges are 4 kV to 161 kV for distribution and 230 kV – 760 kV for transmission. Scaling to these voltage and power levels poses a significant challenge. However, the emergence of applications such as HVDC Lite [47] from ABB suggests that these applications may also prove to be viable.

3.2.1 MODES OF OPERATION

The TACC operates in one of two modes. Active mode is when the augmented asset is operating with the enhanced control capability. The fail-normal mode is a bypass mode that returns the asset and the grid to its original state. The fail-normal mode ensures no degrading of the system reliability.

3.2.1.1 ACTIVE MODE

The active mode of operation is when the converter is providing a power conditioning interface between the asset and the grid. This mode of operation provides dynamic grid control.

The main building block for the TACC can be reduced to a simple AC chopper circuit shown in Figure 3.2. The chopper is inserted between the AC line and the existing grid asset and is generally controlled with a constant duty cycle D at a relatively high switching frequency f . Switches $S1$ and $S2$ are bidirectional switches, while L_f , C_{f1} and C_{f2} are small-sized high frequency filter elements that provide filtering of the high switching frequency components.

The modulated value of the line voltage is applied across the grid asset as D is varied between 0 and 1. As the AC chopper has no low frequency energy storage, the line side of the chopper reflects the low frequency characteristics of the grid asset.

While it may appear at first glance that similar functionality may be obtained with an inverter or a multi-phase matrix converter, this is not the case. It should be recognized that the control objective here is different from an inverter or matrix converter. In the case of an inverter or matrix converter, the main goal is

control of an output voltage. Here, the intent is to reflect the modified asset characteristics on the line side while using the asset within its design specifications.

To provide increased control capabilities of the existing grid asset over and above what can be achieved with simple duty cycle modulation, new techniques need to be employed. Traditionally, single-phase AC choppers have not been used in dynamic control of AC parameters. This is primarily because single-phase converters cannot control the voltages and, or currents at the zero-crossings because of the absence of energy storage. This limitation has been overcome by the use of a novel concept of ‘Virtual Quadrature Sources,’ wherein a quadrature and harmonic source are created simultaneously to allow a shuffling of energy between two virtual sources [49]. Applying this concept to a single-phase AC chopper enables the use of the simple and low device count AC converter for power line conditioning applications. The concept of virtual quadrature sources is discussed in detail in Chapter 4.

3.2.1.2 FAIL-NORMAL MODE

The second mode of operation of the TACC is the fail-normal mode. This mode of operation ensures the grid retains the same level of reliability before and after inclusion of the TACC. Power converters typically low levels of reliability compared to what is required by the power grid. This prevents large-scale use of solutions that utilize power converters in utility applications. The approach proposes the use of a TACC with a safe bypass mode. This mode enables bypass of the converter to allow the system to return to its normal state, should the converter fail.

The bypass is provided by switch S3 as shown in Figure 3.2. S3 is typically a normally closed electromechanical switch or thyristor pair that provides the fail-normal function.

3.3 APPLICATIONS OF THIN AC CONVERTERS

Shunt VAR capacitors and load tap changing transformers are some examples of assets on the grid that provide static control. This section will

discuss the augmentation of these assets using TACCs to realize enhanced control capabilities.

3.3.1 INVERTER-LESS STATCOMs

Shunt VAR capacitors provide leading VAR support on the grid. VAR support is typically required during dynamic conditions, usually to help the system ride through faults. Figure 3.3(a) shows an example of how a TACC can be used with a shunt VAR capacitor (TACC-C) to realize a dynamically controllable VAR compensator [54].

The switches are nominally operated at a frequency f and a duty cycle D and $(1-D)$ as shown in Figure 3.3(a). The TACC can be connected between the shunt VAR capacitor and the grid to realize both a buck and a boost cell, as shown.

The buck cell can provide linear control of the capacitance of the shunt VAR capacitor. At a duty cycle D , the effective net capacitive impedance on the input is seen to be $X_{\text{eff}} = \frac{X_C}{D^2}$. The capacitive VARs drawn can thus be varied from zero to the maximum nominal value.

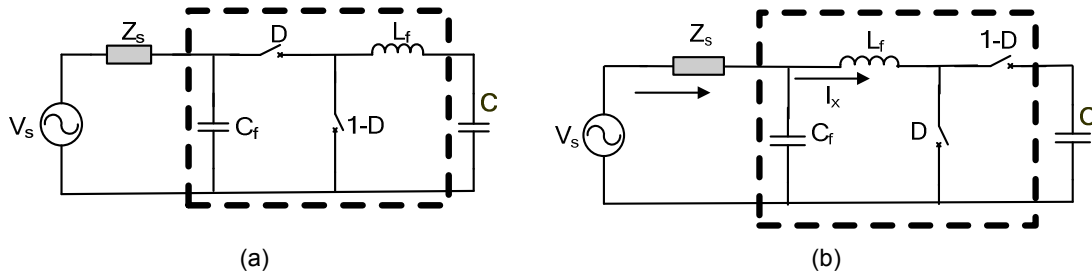


Figure 3.3: TACC-C: (a) buck cell, (b) boost cell

The boost cell can provide an increase in the net capacitance (as seen from the input). Varying D between 0 and 1 changes the capacitance seen at the input $C_{\text{eff}} = \frac{C}{(1-D)^2}$.

Additional control capabilities have been shown to be possible using the principle of virtual quadrature sources discussed in Chapter 4.

3.3.2 CONTROLLABLE NETWORK TRANSFORMERS

An important application for TACCs is to provide enhanced control capabilities to the large number of LTCs that are used in the distribution networks. Slow electromechanical tap changers are adjusted under dispatch commands or seasonally to accommodate changing load profiles. As utilities move toward higher levels of dynamic loading in their networks the issue of reliability and controllability becomes very important. Figure 3.4 shows a TACC deployed with a typical LTC to implement a controllable network transformer or TACC-T. It is highly desirable to simultaneously control the node voltage and the branch currents in a meshed network. The augmentation of the LTC with the TACC provides the control of node voltage and not branch currents. The details of enhanced control capabilities of the TACC-T are discussed in Chapter 5.

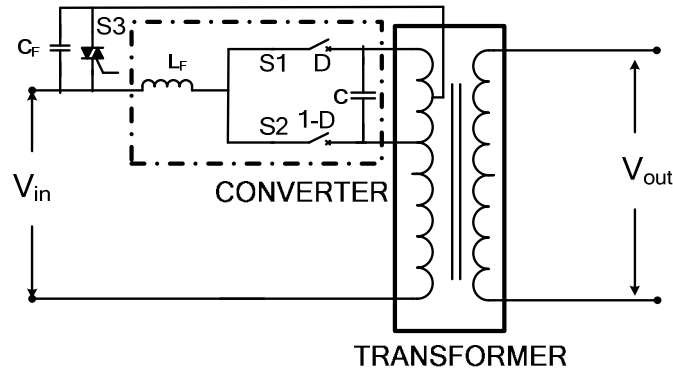


Figure 3.4: Augmentation of an existing LTC with a TACC - TACC-T

The TACC-T output voltage can be dynamically controlled in amplitude to provide linear control of the node voltage. The range of control that the TACC-T provides is determined by the tap ratio, which in turn dictates the rating of the AC - AC converter. The TACC-T is different from a conventional LTC as it provides linear and dynamic control over the desired range of the node voltage, whereas an LTC provides control of the node voltage at discrete set-points with a response time of a couple of cycles.

3.4 CONCLUSION

A novel concept to realize dynamic grid control of existing grid assets has been presented in this chapter. The concept of thin ac converters proposes augmenting existing grid assets with a thin converter to realize smart and controllable grid assets. This can be achieved at a much lower cost than was previously possible. Examples of TACCs include controllable network transformers (CNT) and inverter-less STATCOMs (ILSTATCOM).

The CNT is realized by augmenting an existing LTC with a TACC. The augmented converter can dynamically control the voltage magnitude on the output of the transformer. The device can also provide linear control of the voltage.

The ILSTATCOM is a dynamically controllable VAR compensator that is realized by augmenting a shunt VAR capacitor with a TACC. This device has functionalities comparable to a STATCOM.

CHAPTER 4

PRINCIPLE OF VIRTUAL QUADRATURE SOURCES

4.1 INTRODUCTION

The concept of virtual quadrature sources (VQS) is presented in this chapter. This concept is illustrated using a low-cost AC converter that is robust, has minimal component count, and that is normally limited in control capability. By applying the concept of VQS, the converter is shown to have control of the phase-shift and, or harmonic control without requiring multiple sources or energy storage elements. The approach is seen to have a simple method of implementation that can be used to enhance the control capabilities of devices such as controllable network transformers and inverter-less active filters.

4.2 METHODS OF AC POWER CONVERSION

Control of magnitude, phase angle, and harmonic content can be achieved using a power converter. Power converters can synthesize the desired voltage (current) from available voltages (currents) through the use of pulse width modulation techniques. In the most general case, the synthesized voltage has a different frequency and amplitude in relation to the incoming voltage, e.g., variable speed motor drives. In such applications the power converter of choice is either an AC-DC-AC rectifier-inverter system or an AC-AC matrix converter system, as shown in Figure 4.1(a) and (b).

A common requirement for these systems is the need for an energy storage element or source that provides an outer boundary or envelope within which the desired voltage can be synthesized. In the back-to-back converter the energy storage element is the DC link capacitor, while in the matrix converter the additional phases act as energy storage.

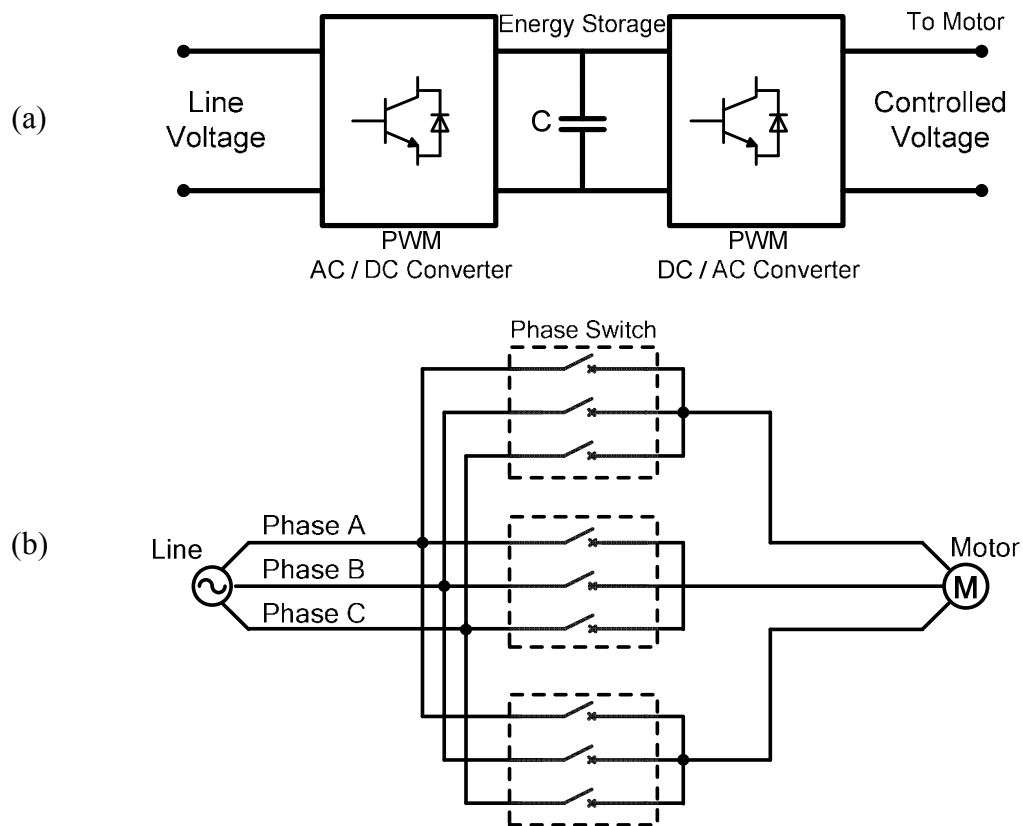


Figure 4.1: AC power conversion, (a) rectifier-inverter system, (b) matrix converter

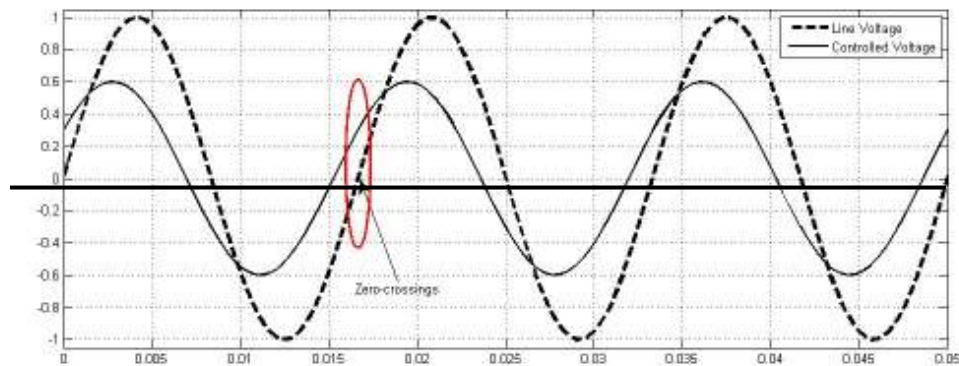


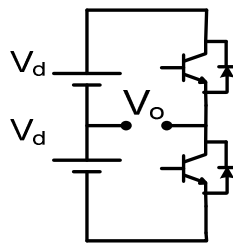
Figure 4.2: Illustration of energy requirements at the zero-crossings of the line voltage

Line conditioning applications usually involve a change in the amplitude, phase angle, and, or harmonics of the incoming voltage, but no change in line frequency. Applications include voltage regulation, power factor or harmonic control, and injection of missing voltage. Control of phase angle and, or harmonics requires the addition of a finite voltage on the output when the line

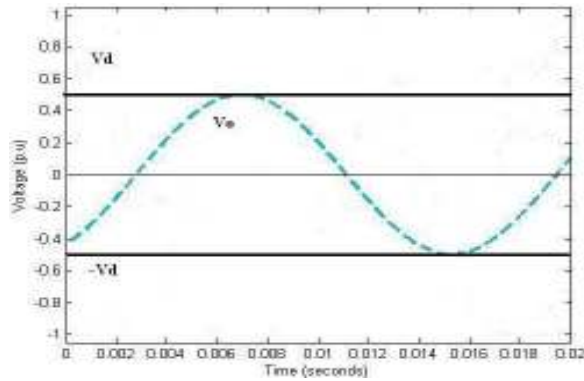
voltage is undergoing a zero-crossing. This is illustrated in Figure 4.2, where energy is needed at the zero-crossings of the input voltage to synthesize a finite phase-shift between the input and output.

4.2.1 INVERTER-BASED APPROACH

The region within which voltage can be synthesized in an inverter is defined by the DC, as shown in Figure 4.3. The desired output voltage can be synthesized anywhere within the boundary defined by the supply voltages.



(a)



(b)

Figure 4.3: Inverter based system, (a) schematic, (b) region of achievable output voltage

This basic principle is what is used in the control of all voltage source converters, e.g. FACTS devices [49].

4.2.2 DIRECT AC-AC CONVERTERS

Direct AC-AC conversion can be done on a three-phase and single-phase basis, using matrix converters and AC choppers respectively. The former is a complex converter comprising of nine bidirectional AC switches that interconnects the three phases. The AC chopper has a total of six as switches, two per-phase and no energy storage. The AC chopper however is limited in functionality.

4.2.2.1 THREE-PHASE APPROACH

Inverters and matrix converters can be used to synthesize an output voltage of variable frequency. While it may appear that matrix converters do not require

bulk energy storage in the form of DC capacitors, they do equivalently need additional sources as well as switches to interconnect the available phases to the output terminal [50], [51].

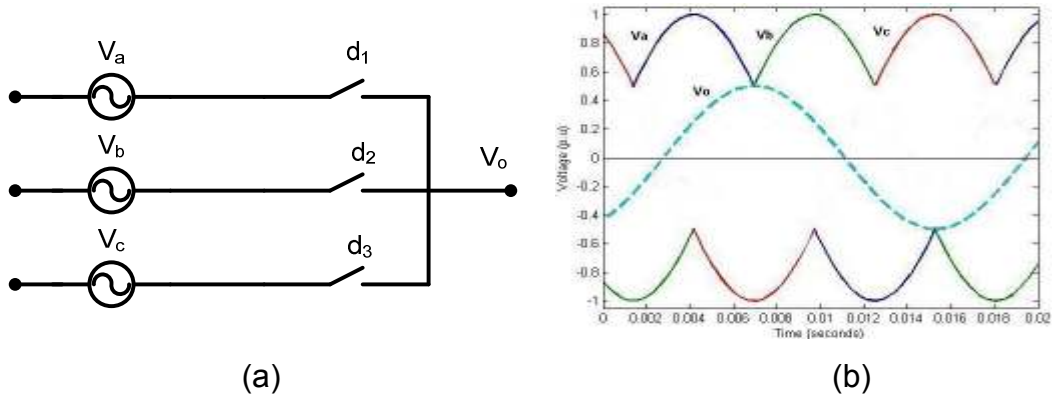


Figure 4.4: Matrix converters (a) single output line (b) region of achievable output voltage

Figure 4.4 shows a schematic of a single output line of the matrix converter and the boundary within which the output voltage can be synthesized. The matrix converter can provide control of phase angle and, or harmonic content of the output voltage. The matrix converter cannot however be used to realize the TACC concept as it does not have the ability to reflect the existing asset value on the line.

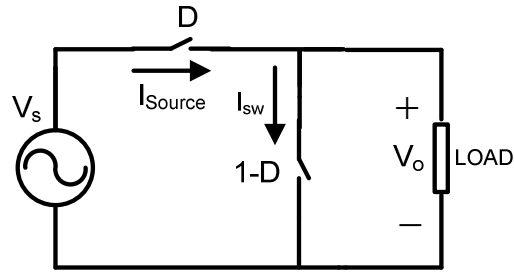
The single-phase approach uses an AC chopper for power conversion. The chopper uses no bulk energy storage elements and has no cross-coupling between phases. The single-phase AC chopper is discussed in the following section.

4.2.2.2 SINGLE-PHASE APPROACH

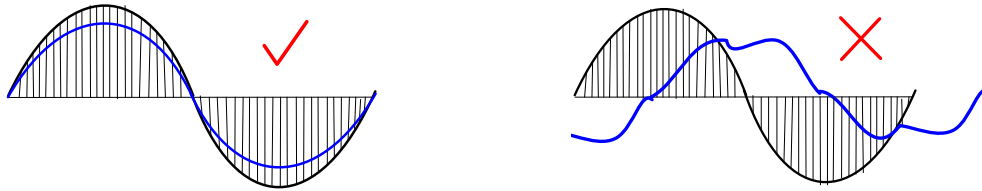
The simplest form of AC line conditioner is the AC chopper shown in Figure 4.5(a). It has a low component count and no stored energy. However it is limited in the ability to control the output voltage. The converter can synthesize an output voltage V_o from the source voltage V_s using fixed-frequency PWM techniques with the relation,

$$V_o = D \cdot V_s \quad (4.1)$$

Here, V_s is the voltage at the input and D is the duty cycle.



(a)



(b)

Figure 4.5: (a) Single-phase AC chopper, (b) achievable output voltage

Converter operation results in a scaled version of the incoming line voltage, i.e., V_o falls within the envelope defined by V_s and zero volts. It has not been considered possible to use this simple circuit to control the phase-shift and, or harmonic content of the output voltage. This is because control of these parameters requires a finite voltage at the zero-crossing points of the incoming line voltage.

The novel principle of virtual quadrature sources presented in this chapter allows the use of this minimal circuit topology to synthesize a phase-shifted and, or harmonic-modified output voltage with no bulk energy storage.

4.3 CONCEPT OF VIRTUAL QUADRATURE SOURCES

The principle of virtual quadrature sources uses voltage synthesis techniques to realize controllable AC components of voltage and, or current. Practical implementation of this concept has been shown possible using a simple modulation strategy. The synthesis and implementation principles and techniques will be discussed in the following sections.

4.3.1 VIRTUAL QUADRATURE SOURCES USING VOLTAGE SYNTHESIS

Assume that the incoming line voltage V_{in} is aligned with the direct or d-axis. The desired output voltage V_O^* is phase-shifted by angle Φ with respect to the input. The output voltage V_O^* is the phasor sum of two voltages, a direct component V_{dO}^* and a quadrature component, V_{qO}^* as shown in Figure 4.6(b).

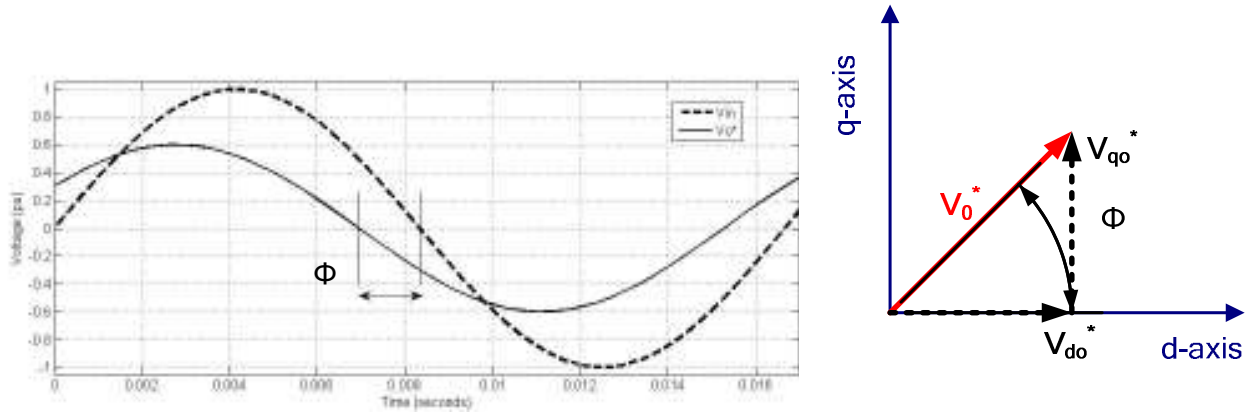


Figure 4.6: (a) Input and output voltage, (b) phasor representation of the input and output voltages

As discussed earlier, it has so far not been possible to synthesize a phase-shifted output voltage V_O^* using the AC chopper and conventional voltage synthesis and modulation techniques.

One way to think about synthesizing the phase-shifted voltage is by the addition of two quadrature sources to a scaled component of the input voltage V_{dO}^* . The first is a quadrature component at the fundamental frequency which when summed with V_{dO}^* results in the desired phase-shifted output voltage. The second quadrature component needs to ensure that the sum of all three components satisfies the physical constraints on the system at all times. One way to realize this is using a quadrature source at an odd harmonic, say the third harmonic frequency. The process of summing the three sources is shown in Figure 4.7(a) – (c).

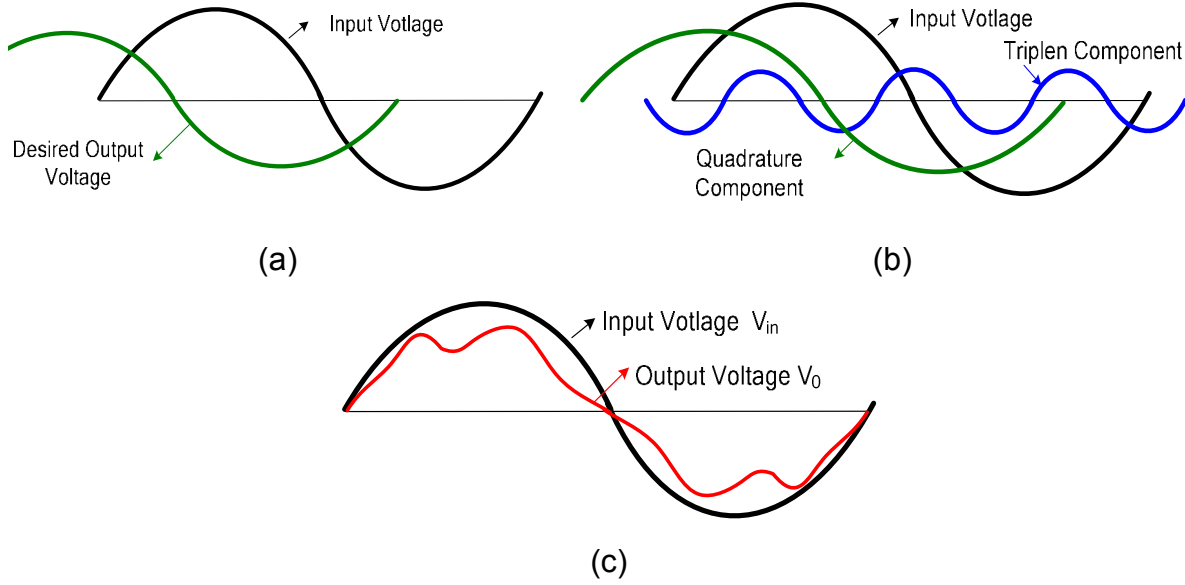


Figure 4.7: Voltage synthesis: (a) input and desired output voltage, (b) addition of triplen and quadrature components, (c) resultant output voltage

The resultant voltage V_o is seen to lie entirely within the envelope provided by the incoming voltage V_{in} . The phase-shifted voltage synthesized therefore has three components, a direct component at the fundamental frequency, a quadrature component at the fundamental frequency, and a quadrature component at the third harmonic frequency.

The two components that have been added to the d-axis component of the input voltage can be desirable or undesirable based on the application. In cases where the third harmonic component is undesirable a filter or trap may be used.

Practical implementation of the voltage synthesis technique will be discussed in the following section.

4.3.2 PRACTICAL IMPLEMENTATION OF VQS - EVEN HARMONIC MODULATION

The modulation strategy used to realize the desired quadrature sources is formulated by analytically considering the physical constraints on the system. The input and output voltages V_{in} and V_o are as given by Equations 4.2 and 4.3.

$$V_{in} = V_m \sin \theta \quad (4.2)$$

$$V_O = V_{do} \sin \theta + V_{qo} \cos \theta + V_3 \sin(3\theta + \varphi_3) \quad (4.3)$$

Here, V_m is the peak of the input voltage, V_O is the output voltage, V_{do} , V_{qo} , and V_3 are the direct, quadrature, and third harmonic components of the output voltage, and φ_3 is the angle of the third harmonic.

One can then set up the physical constraints as follows:

$$0 < V_O(\theta) < V_m \sin \theta \quad 0 < \theta < \pi \quad (4.4)$$

$$0 > V_O(\theta) > V_m \sin \theta \quad \pi < \theta < 2\pi \quad (4.5)$$

Matching the input and desired output voltages at $\theta = 0$ gives

$$V_{qo} = V_3 \sin \varphi_3 \quad (4.6)$$

If the variable to be controlled is V_{qo} , then setting $\Phi_3 = \pi/2$ yields the minimum level of third harmonic that must be injected to realize the desired control. This results in computation of the duty cycle as a function of time (angle) as,

$$D(\theta) = \frac{V_0^*}{V_m} = \frac{V_{do}}{V_m} + \frac{V_{qo}}{V_m} \cot(\theta) - \frac{V_3 \cos 3\theta}{V_m \sin \theta} \quad (4.7)$$

The duty cycle has a DC component and a time varying component. The expression for $D(\theta)$ can be simplified as,

$$D(\theta) = \frac{V_{do}}{V_m} + \frac{2V_{qo}}{V_m} \sin 2\theta \quad (4.8)$$

This surprising finding suggests that a simpler real-time modulation strategy may be possible, that will provide the same degree of control that can be achieved using the voltage synthesis technique described above.

By way of an example, consider the control reference voltage $D(\theta)$ to have a DC component (K_0) to synthesize the desired V_{do}^* and a second harmonic of amplitude K_2 and phase angle φ_2 . Assume sine triangle pulse width modulation is used.

$$D(\theta) = K_0 + K_2 \sin(2\theta + \varphi_2) \quad (4.9)$$

The resulting chopper output voltage is obtained by multiplying $D(\theta)$ with the input voltage V_{in} ,

$$V_0 = V_m \sin \theta (K_0 + K_p \sin(2\omega t + \varphi_2)) \quad (4.10)$$

$$= V_m K_0 \sin \theta + V_m \frac{K_2}{2} \cos(\theta + \varphi_2) - V_m \frac{K_2}{2} \cos(3\theta + \varphi_2) \quad (4.11)$$

Equation 4.11 clearly shows the three components of the output voltage, V_{do} , V_{qo} , and a third harmonic component V_3 at an angle φ_3 . Further, it is possible to use additional even harmonics in the modulation signal, such as the fourth harmonic to generate a desired V_{qo} and additional components at the third and fifth harmonic frequencies.

This clearly shows that there are two possible control variables. The first is the phase angle, which is a result of the phasor sum of the quadrature sources at the fundamental frequency. The second control variable is the quadrature source(s) at the harmonic frequencies. The ability to generate controllable harmonic voltages opens up an entire slew of applications in harmonic compensation.

4.3.2.1 CONTROL OF PHASE ANGLE

Phase angle control is achieved by controlling K_0 , K_2 and φ_2 . The effect of each variable on the phase angle can be seen from equation 4.12 and equation 4.13.

$$|V| = V_m \sqrt{\frac{K_2^2}{4} - K_0 K_2 \sin \varphi_2 + K_0^2} \quad (4.12)$$

$$\varphi = \tan^{-1} \left[\frac{\frac{K_2}{2} \cos \varphi_2}{K_0 - \frac{K_2}{2} \sin \varphi_2} \right] \quad (4.13)$$

Using equations (4.12) and (4.13) and varying K_0 , K_2 and φ_2 , an arbitrarily phase-shifted voltage at the fundamental frequency can be synthesized. The control range is defined for D ranging between 0 and 1.

The impact of one of the three variables is shown in Figure 4.8. As the phase angle of the second harmonic component of the modulation signal ϕ_2 is varied the magnitude and phase of V_o can be controlled.

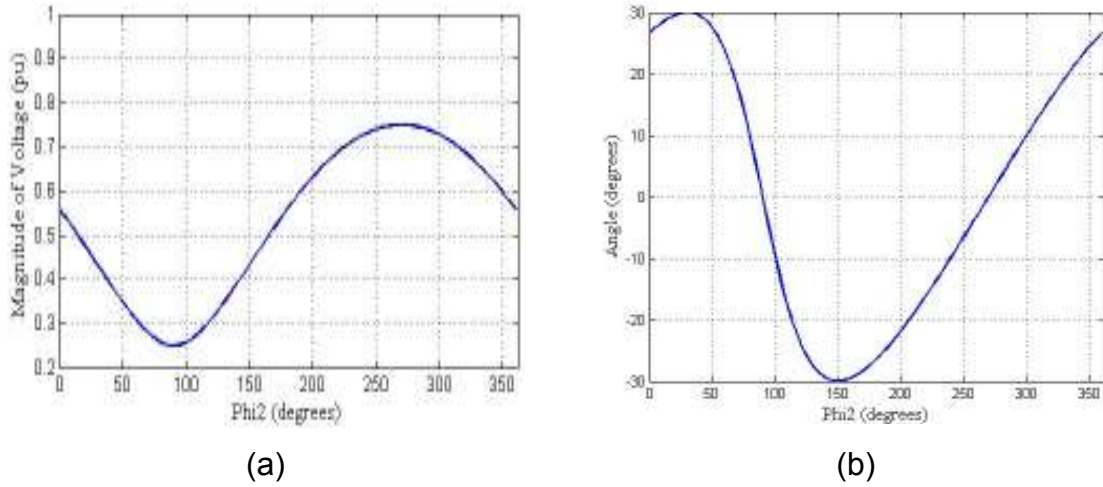


Figure 4.8: Variation of of (a) magnitude (b) phase with Φ_2

The control contours illustrate the maximum achievable phase angle and the control range for the voltage magnitude. This is achieved by setting $K_0 = K_2 = 0.5$, and varying ϕ_2 . The most desirable feature is the linear control region with ϕ_2 as a control variable. The achievable control region in the d-q plane is illustrated in Figure 4.9.

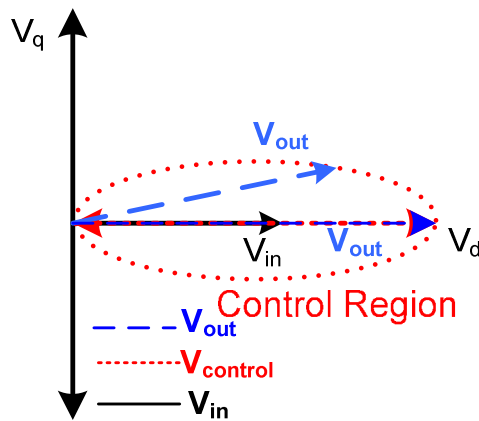


Figure 4.9: Control region for single-phase AC chopper

An example to illustrate the phase-shift of the output voltage at the fundamental frequency is shown in Figure 4.10(a), and (b). The plot shows the maximum achievable phase-shift using this technique, where $|V_d| = 0.5\text{pu}$, $|V_q| = 0.25\text{pu}$, and $|V_3| = 0.25\text{pu}$.

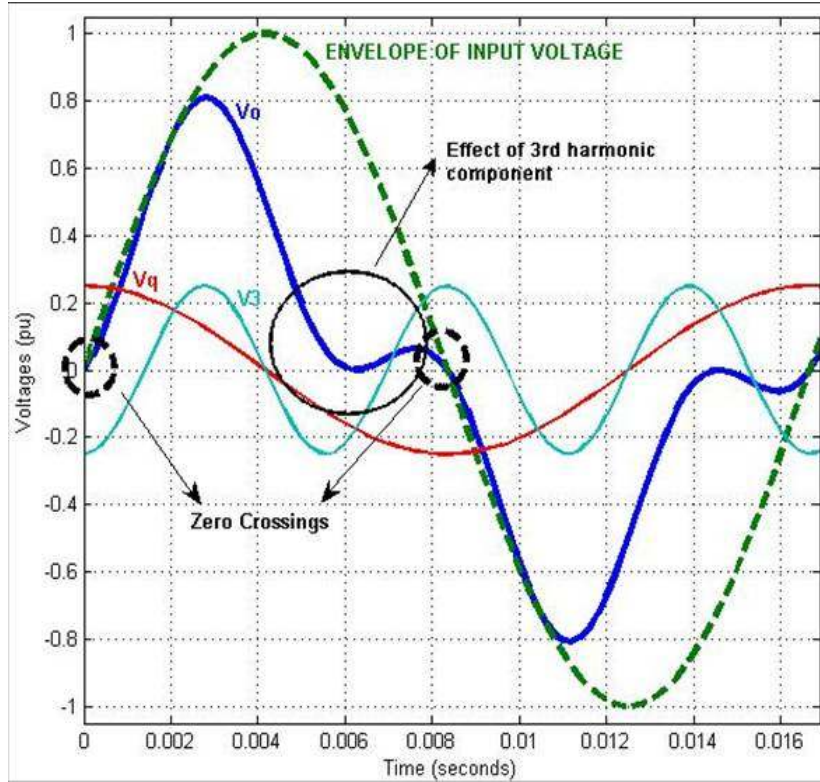


Figure 4.10: (a) Phase angle control

Figure 4.10(a) shows the different components that are used in generating the desired phase-shifted output voltage at the fundamental frequency.

The input voltage and phase-shifted output voltage are shown in Figure 4.10(b). The phase-shift between the input and output voltage is close to 30 degrees.

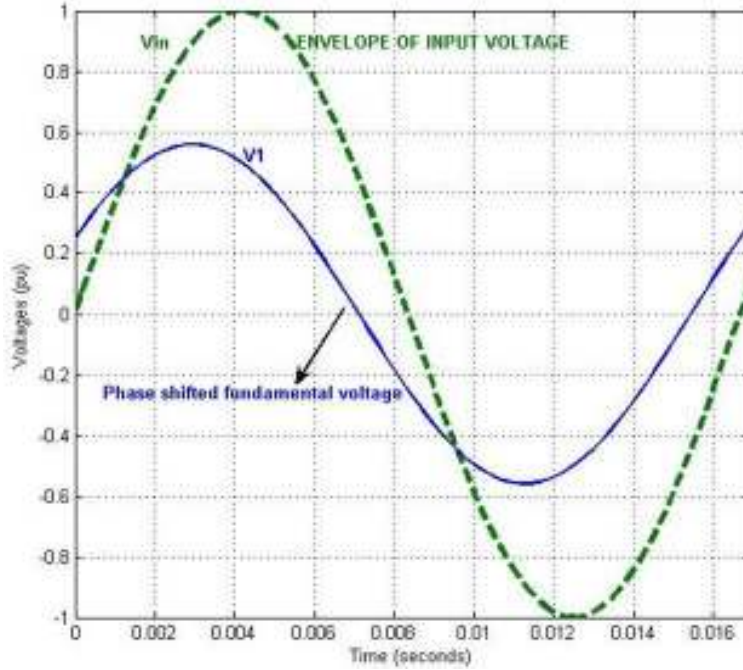


Figure 4.11: (b) Input and output voltage

Phase angle control can be achieved using the above principle without any large DC capacitors or inductors, and does not require the use of a DC-ac inverter. It is important to mention the need for filtering of high frequency PWM. Further, the resulting 3rd harmonic components may need to be filtered in some applications.

4.3.2.2 CONTROL OF HARMONICS

Control of the quadrature sources at the harmonic frequencies can be achieved using even harmonic modulation. A modulation signal with a DC and second harmonic component will yield a single harmonic voltage source at the 3rd harmonic frequency. The effect of the control variables K_0 , K_2 and ϕ_2 on the third harmonic component of the output voltage can be seen from Equation 4.14.

$$V_3 = -\frac{K_2}{2} \cos(\omega t + \phi_2) \quad (4.14)$$

The magnitude of the third harmonic component is dependant on the quadrature component generated at the fundamental frequency. This is because there is interdependency between the two sources that results in the shuffling of

energy between the sources, resulting in an output voltage that satisfies the physical constraints on the system. Figure 4.12 shows an example of an arbitrarily phase-shifted third harmonic component with $|V_d| = 0.73\text{pu}$, $|V_q| = 0.13\text{pu}$, and $|V_3| = 0.15\angle 30^\circ\text{pu}$.

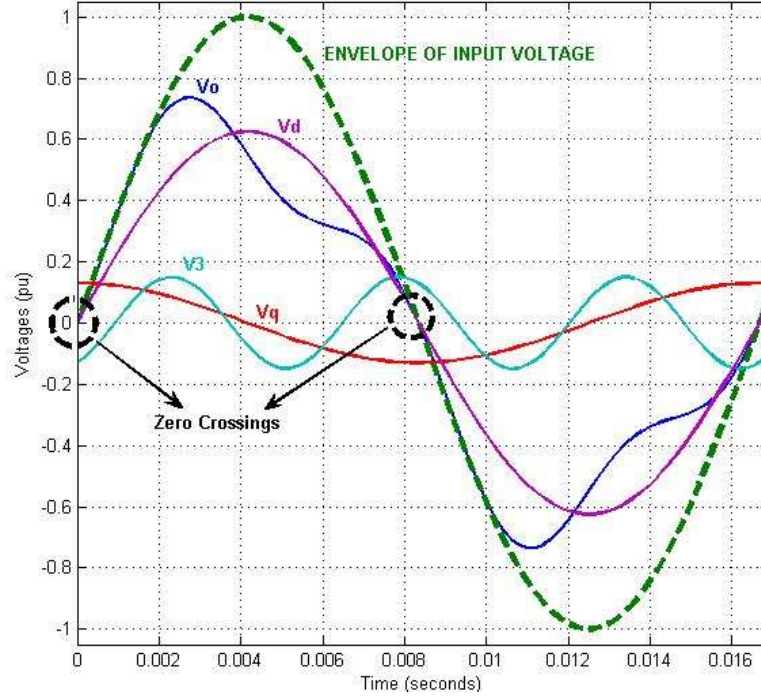


Figure 4.12: Harmonic control

The idea can be further extended to compensate for more harmonics. The modulation signal can have multiple even harmonics, which when multiplied with the input voltage results in phase and amplitude controllable harmonic components. Equation 4.15 is an example of a modulation signal with multiple even harmonics.

$$D(\theta) = K_0 + K_2 \sin(2\theta + \varphi_2) + K_4 \sin(4\theta + \varphi_4) + \dots \quad (4.15)$$

The output voltage generated as a result of the modulation signal in equation 4.15 will have quadrature components at the fundamental, third, and fifth harmonic frequencies.

Application of this concept in harmonic compensation will be discussed in Chapter 5.

4.3.3 SINGLE-PHASE AC CHOPPER

Even Harmonic Modulation will be used to demonstrate the concept of virtual quadrature sources using a single-phase AC chopper shown in Figure 4.13. Control of phase angle at the fundamental as well as the ability to generate arbitrarily phase-shifted harmonics will be demonstrated.

The first set of simulation results illustrates the maximum phase-shift that can be achieved using this modulation technique. A third harmonic trap has been included to trap the undesirable third harmonic voltage, which is a by-product of the proposed technique.

Inclusion of the third harmonic trap is through a transformer, such that the magnetizing inductance is used as the inductance for the trap. The leakage inductance of the transformer works as the filter inductance. Inclusion of the transformer facilitates appropriate selection of a commercially available capacitor, i.e., a capacitor that can has the ripple current capability required for this application.

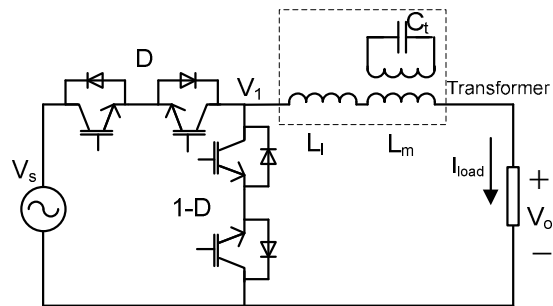


Figure 4.13: AC chopper with third harmonic trap

The converter has been simulated at an input voltage of 1400 Vrms. The maximum phase-shift that can be achieved is 30 degrees. Figure 4.14 shows the input and output voltage of the AC chopper with the phase-shifted output voltage at an angle of 25 degrees with respect to the input. The loss of 5 degrees is because of the third harmonic trap.

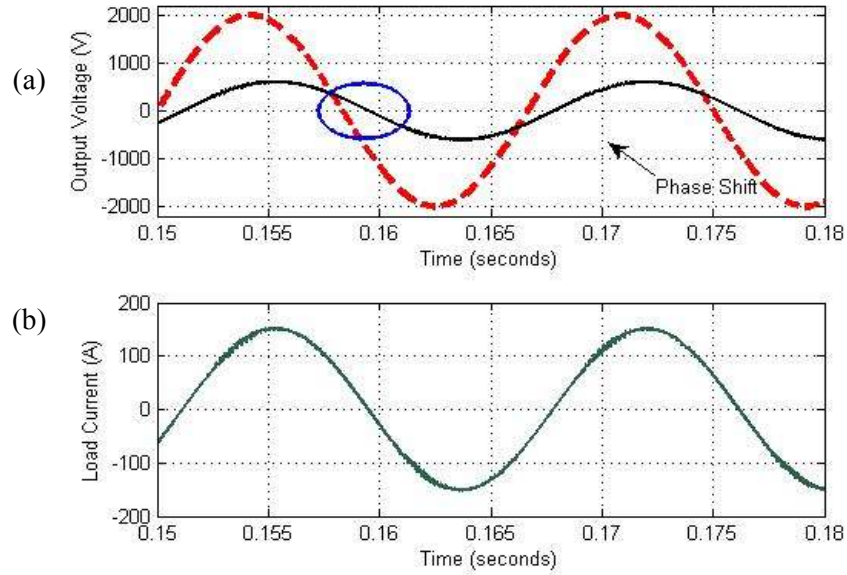


Figure 4.14: (a) Input and output voltage (b) load current

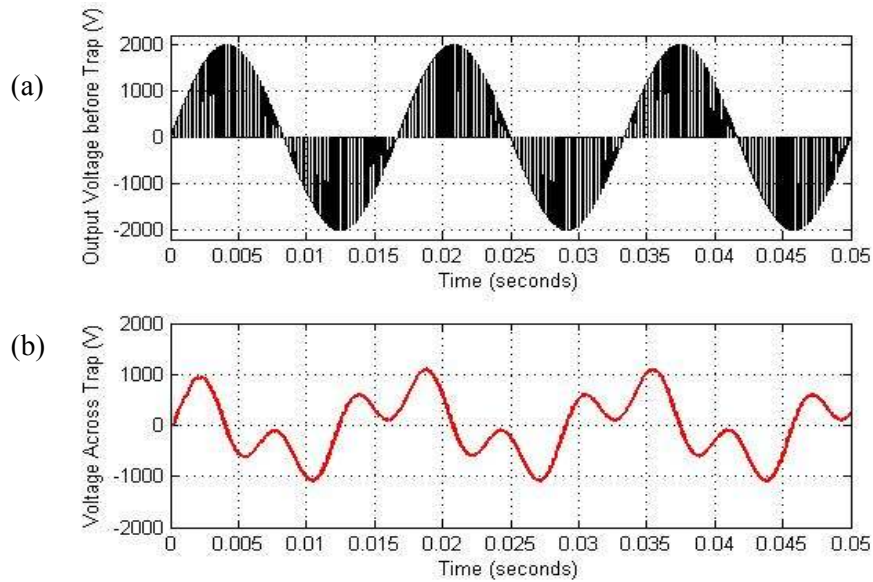


Figure 4.15: (a), Voltage across switch, V_1 (b) voltage across third harmonic trap

The voltage, V_1 at the output of the two-switch pair is shown in Figure 4.15(a). This voltage has a fundamental component of 860 V and a phase-shift of 30 degrees. The voltage across the third harmonic trap is shown in Figure 4.15(b).

Demonstration of the synthesis technique to generate multiple harmonics with controllable magnitudes and phase angles is presented in Figure 4.16 and

4.17. The AC chopper has been controlled to generate third and fifth harmonics. The modulation signal there has DC, second, and fourth harmonic components.

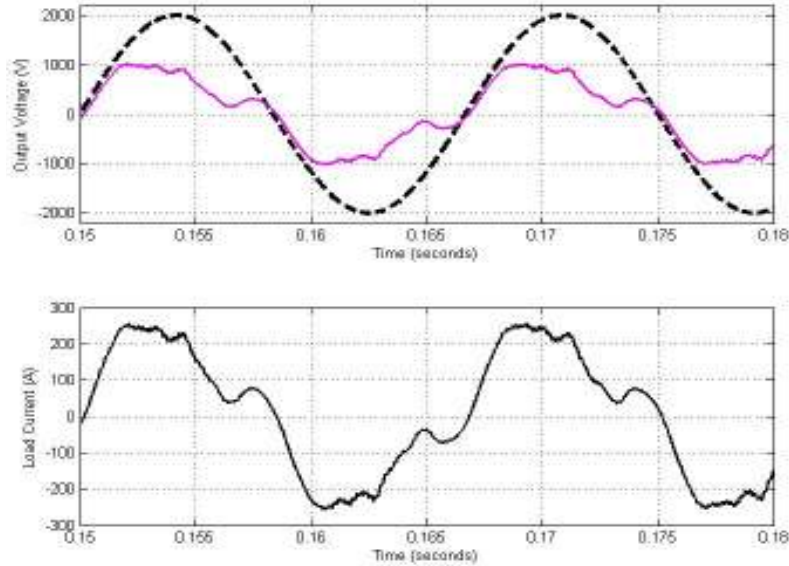


Figure 4.16: (a) Input and output voltage (b) load current

The output voltage and load current are shown in Figure 4.16(a) and (b). The output voltage lies within the boundary of the input, as enforced by the physical constraints on the system. The load current is seen to have harmonics at the third and fifth harmonic frequencies. The fifth harmonic voltage source is 11% of the input voltage at an angle of -78 degrees. The fifth harmonic voltage has been controlled to 6.25% of the input at an angle of -60 degrees.

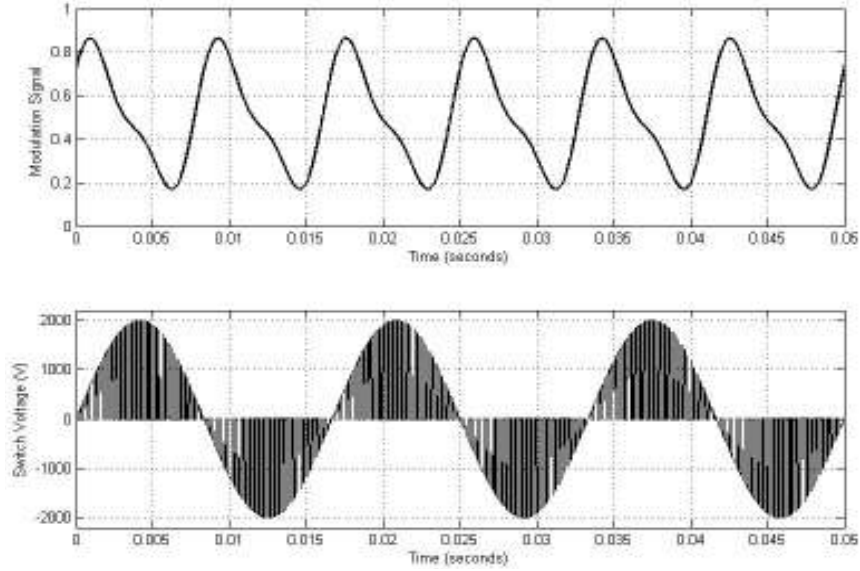


Figure 4.17: (a) Modulation signal (b) voltage across switch, V_1

The switch voltage and modulation signal are shown in Figure 4.17(a) and (b). The following are the parameters used in the modulation signal,

$$K2 = 0.3 \angle 30^\circ$$

$$K4 = 0.1 \angle 45^\circ$$

The ability to generate arbitrary harmonics is a powerful tool. It is important to mention the limits within which this is possible. The modulation signal is limited between 0 and 1. This means the sum of the even harmonic components need to be less than or equal to the DC component of the modulation signal. This limits the magnitude of harmonics that can be generated using this technique. Leveraging this technique using novel circuit topologies will be discussed in Chapter 5.

4.4 CONCLUSION

The principle of virtual quadrature sources is a novel method for controlling the phase angle and, or harmonic content of a voltage (current) with no bulk energy storage. The technique opens up the possibility of providing control of AC parameters on a single-phase basis with no bulk energy storage. The application areas for this principle can be split into two. The first set of

applications targets areas where control of phase angle of the line voltage or current is important. One such example is the control of power flow in power networks. The second set of applications utilizes the controllable harmonic voltages to provide harmonic compensation. Applications of this novel principle will be presented in the following Chapter 5.

Practical implementation of the principle of virtual quadrature sources has been shown possible using a simple real-time modulation strategy. The simplicity of the modulation strategy lends itself to the elegant concept that has been proposed.

CHAPTER 5

APPLICATIONS OF VIRTUAL QUADRATURE SOURCES

5.1 INTRODUCTION

Applications of the concept of virtual quadrature sources will be discussed in this chapter. The applications are divided into two; the first includes applications where control of the amplitude and phase angle of the voltage at the fundamental frequency is desired. The second set of applications considers the control of harmonic components in the voltage or current as the control objective.

The CNT [52] is discussed as a controllable network element that provides simultaneous control of voltage magnitude and phase angle. The basic principle for voltage magnitude control and topology is briefly discussed in Chapter 4. The concept is extended to phase angle control using VQS.

Applications that demonstrate harmonic and VAR compensation capabilities of the single-phase AC chopper using VQS will be discussed. Details on different types of filters will be presented with by simulation and experimental results.

5.2 CONTROLLABLE NETWORK TRANSFORMERS

The conventional approach to network operation of static assets is through the use of off-line optimal power flow and state estimation techniques. These techniques provide the system operator with parameters that are used to control generator excitation, LTC transformers, and shunt VAR compensation capacitors. These operating points are selected to ensure constraints on the system are not violated, i.e., voltage regulation at the buses between 0.95 pu, and 1.05pu, and line current does not exceed thermal limits. In a highly interconnected meshed network this represents a very challenging control problem because of the interdependencies between parameters. The non-trivial

nature of the control problem has so far discouraged implementation of real-time controllers in meshed networks.

The controllable network transformer (CNT) proposes augmentation of an existing load tap changing transformer to provide dynamic, vernier control of voltage magnitude and phase angle simultaneously. The following sections will discuss implementation of the CNT in meshed systems and propose localized control techniques that will allow simultaneous control of voltage magnitude and phase angle.

5.2.1 CNT – THE BASICS

The CNT is shown in Figure 5.1. The device is realized by augmenting a LTC with a fractionally rated converter. Control of voltage magnitude is typically required over a small range in power networks, usually about $\pm 10\%$ of the nominal voltage. The CNT is therefore designed to control voltage magnitudes over this range.

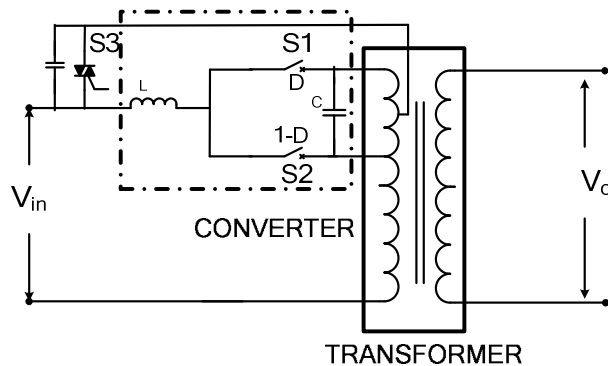
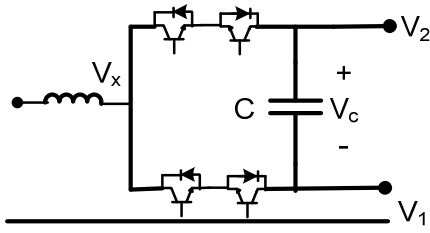
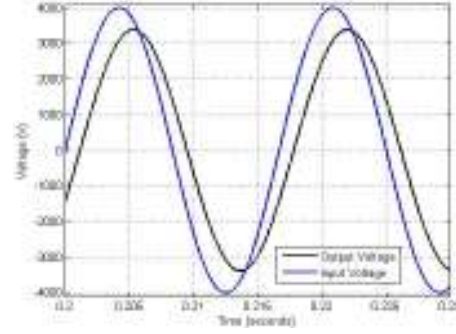


Figure 5.1: Controllable network transformer

Basic operation of the CNT for linear control of voltage magnitude has been briefly discussed in Chapter 3.



(a)



(b)

Figure 5.2: (a) AC chopper, (b) Arbitrarily phase-shifted output voltage

Table 5.1: Modes of operation for the CNT

Mode	Switch State	Duty Cycle 'D'	Output Voltage V_0 (pu)
1	S1 ON	$D = 0$	1.1
2	S2 ON	$D = 1$	0.9
3	S1 ON/S2 ON	$D = 0.5$	1.0

The rating of the AC chopper is dictated by the control range required for the CNT. By way of example, if the CNT is operating with DC modulation and a tap ratio of $\pm 10\%$, the chopper would be rated at 20% the rating of the transformer.

The modes of operation of the CNT are shown in Table 5.1. For the given example, the output voltage of the CNT can be controlled linearly between 0.9 pu, and 1.1 pu. This provides control of only the magnitude of the voltage. To provide control of phase angle the principle of VQS's is applied. This is realized by applying even harmonic modulation (EHM) to the CNT. The resulting output voltage is a function of the turn's ratio of the tap transformer and the modulation signal.

The output voltage (V_0) of the transformer can be expressed as a function of the input voltage (V_S), modulation signal (D), and tap ratio (N), as shown by equation 5.2.

$$V_S = V_m \sin \omega t \quad (5.1)$$

$$V_0 = (1+N) (1-D) V_S + D (1-N) V_S \quad (5.2)$$

$$D(\theta) = K_0 + K_2 \sin(2\theta + \varphi_2) \quad (5.3)$$

The following example illustrates the control range of the CNT when EHM is used. The AC chopper has been rated at $\pm 10\%$ of the nominal voltage. The range of phase angle control is illustrated in Figure 5.3. The maximum achievable phase-shift for this rating is three degrees. This is significant for control of power flow in large systems.

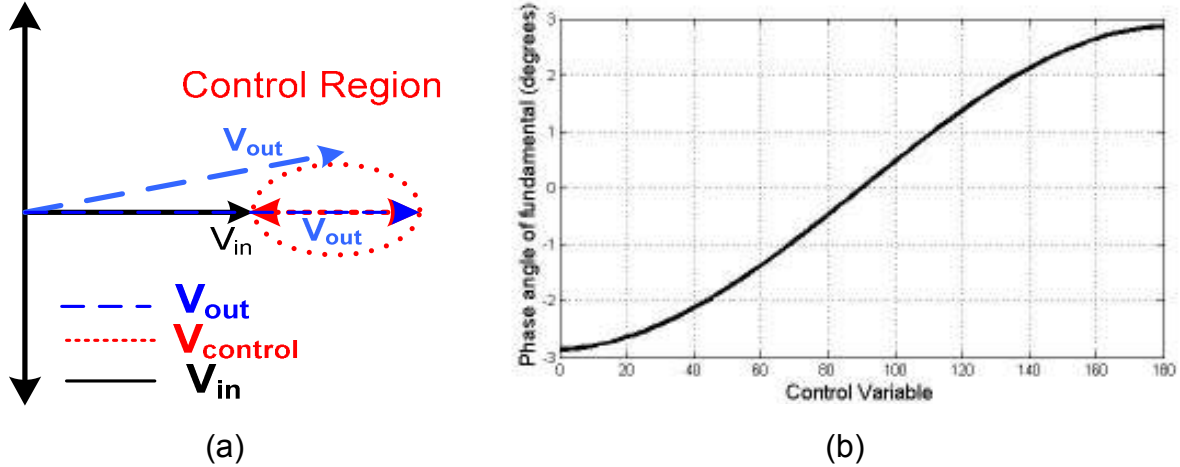


Figure 5.3: (a) Control region (b) variation of the phase angle with the control variable φ_2

Preliminary simulation results for the CNT are presented in the following sections. The AC chopper is rated at $\pm 10\%$ of the nominal voltage, i.e., 20% of the rating of the transformer. The relatively small tap ratio, which implies small-rated converter, has been chosen to demonstrate operation of the CNT. The transformer is simulated at a voltage level of 138 kV. Figure 5.4(a) and (b) show the switch voltage and current, and Figure 5.4(b) shows the actual switching instances. The switch voltage has a peak value of 35 kV and a peak current of 2600A. With $\pm 10\%$ control, the voltage at the output of the transformer can be varied between 151.8 kV and 124.2 kV. The phase angle of the output voltage of the transformer can be varied between ± 3 degrees. Figure 5.4(c) illustrates the input and output voltage of the CNT. The phase-shift generated between the input and output voltage is about 4 degrees. The capacitor voltage of the AC chopper is shown in Figure 5.4(d). The voltage has a peak value of 26 kV, as is expected for the chosen tap ratio.

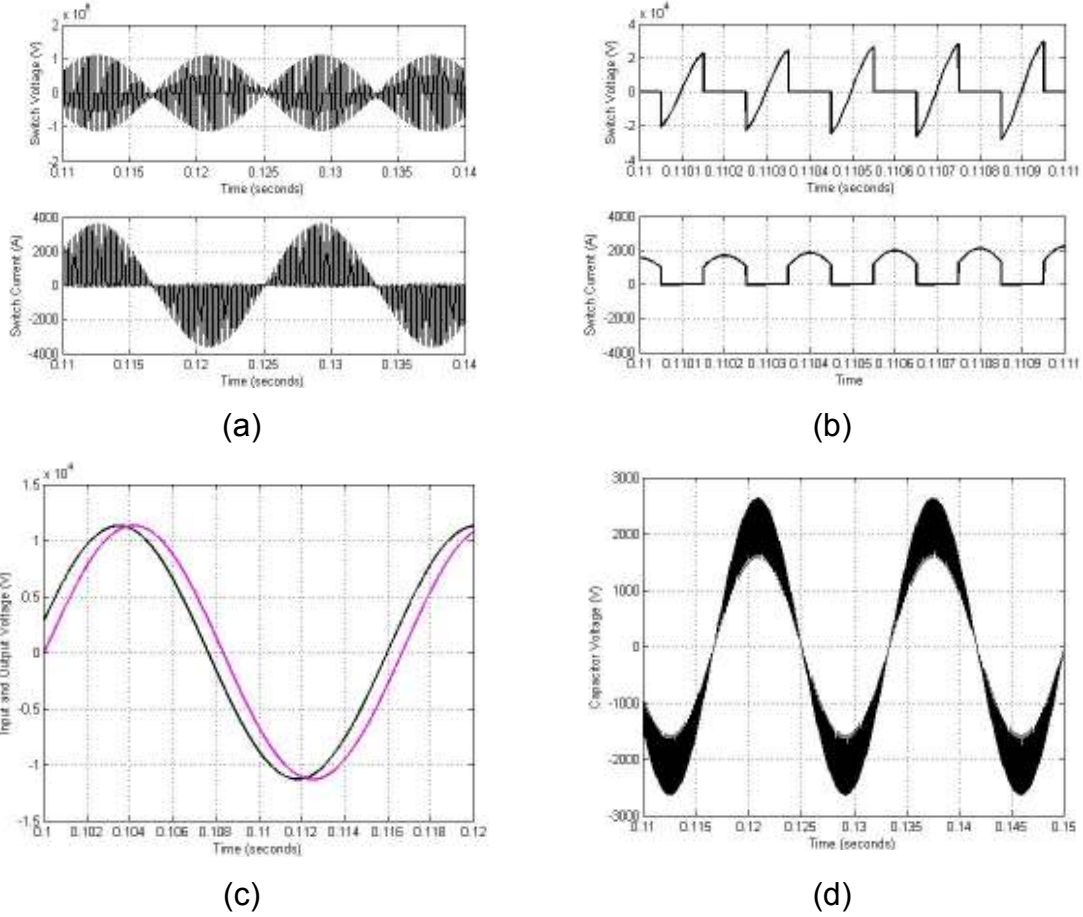


Figure 5.4 (a) Switch voltage and current, (b) switch voltage and current waveforms illustrating switching instances, (c) input and output voltages, (d) capacitor voltage V_c

The simulation results presented so far illustrate the device level operation of the CNT. The ability to generate a controllable voltage on the output is of value when used in a system. System analysis of the CNT will be presented in the following sections.

5.2.2 Two-Bus System Implementation

Functionality of the CNT is tested in a simple two bus, two line system as shown in Fig 5.5. The two-bus system is used to demonstrate the power flow control capability of the CNT. The current in line 1 is uncontrolled and is determined by the line impedance X and the terminal voltages V_1 and V_2 .

$$P = \frac{V_1 V_2}{X} \sin \delta \quad (5.4)$$

Where, $V_1 \angle \delta_1$ = Voltage at Bus 1, $V_2 \angle \delta_2$ = Voltage at Bus 2, and $\delta = \delta_1 - \delta_2$.

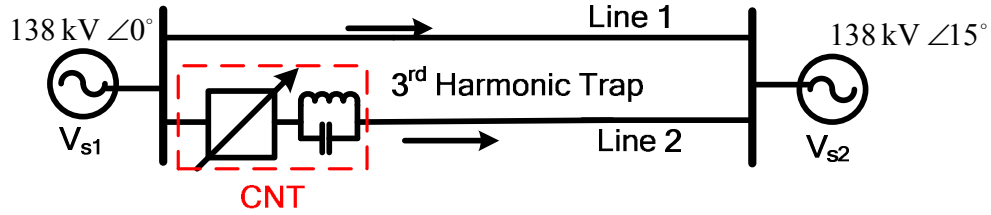


Figure 5.5: Two-bus system

The current in line 2 can be controlled by varying the amplitude and phase angle of the voltage on the output of the transformer. In this example the CNT is controlled to illustrate both an increase and decrease of the current in line 2.

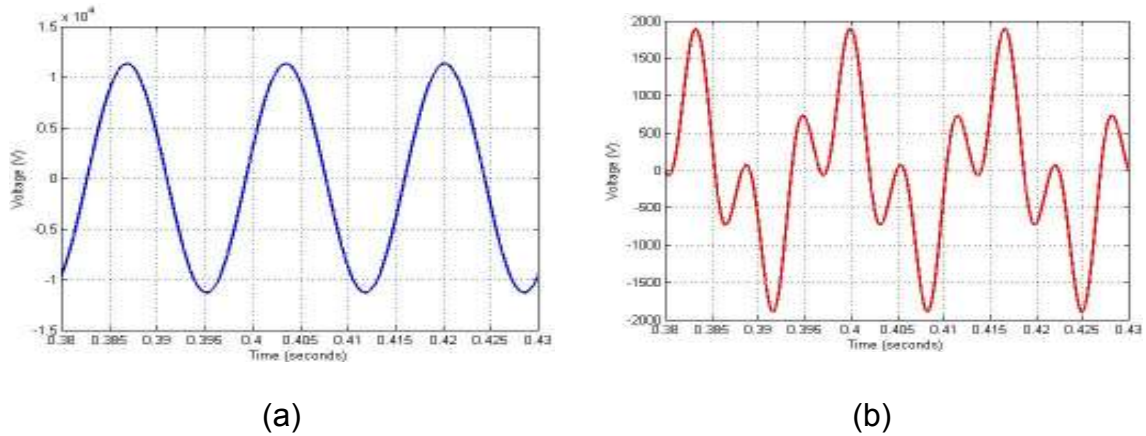


Figure 5.6: (a) Line-voltage after third harmonic trap, (b) Voltage across the third harmonic trap

Simulation results for the two-bus system are shown in Figure 5.6 and 5.7. As discussed in Chapter 4, a by-product of applying VQS to the CNT is the third harmonic voltage synthesized on the output of the CNT. In this example the third harmonic component is eliminated using a series connected harmonic trap. Figure 5.6(a) and (b) show the line voltage after the third harmonic trap and the voltage across the third harmonic trap respectively.

In this simple system the CNT has $\pm 15\%$ control. This translates to ± 5 degrees phase angle control. The rms current can be seen to decrease from

500A to 400A, and then increase to 600A in Figure 5.7. The rms of the line current in line 1 however, remains constant over the entire period as there is no controllable device in line 1.

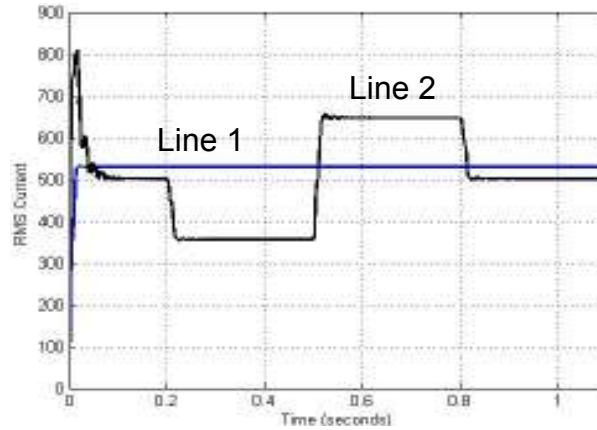


Figure 5.7: RMS of the line current in line 1 and line 2

5.2.3 FOUR-BUS SYSTEM IMPLEMENTATION

Implementation of the CNT in a meshed network will be discussed in this section. The CNT does not provide much value in networks that are radial in structure. This is primarily because the control action and the corresponding effect i.e., change in phase angle and the corresponding change in the line current has a one-to-one correlation in radial networks. This means that a change in the current in one line which is caused by a change in the phase angle does not impact the rest of the system. Also the flow of power in radial systems is dictated by the loads at the consumer end.

The most valuable feature of the CNT is the ability to provide simultaneous control of voltage magnitude and phase angle. This makes the CNT highly effective and desirable in meshed networks because of the high coupling between parameters.

Figure 5.8 illustrates an example of a meshed network. Meshed networks are challenging to control because of the inter-dependence between network voltages and currents. By way of an example, consider a change in current in any line for the five-bus system in Figure 5.8. This change will cause the currents in the remaining lines to redistribute.

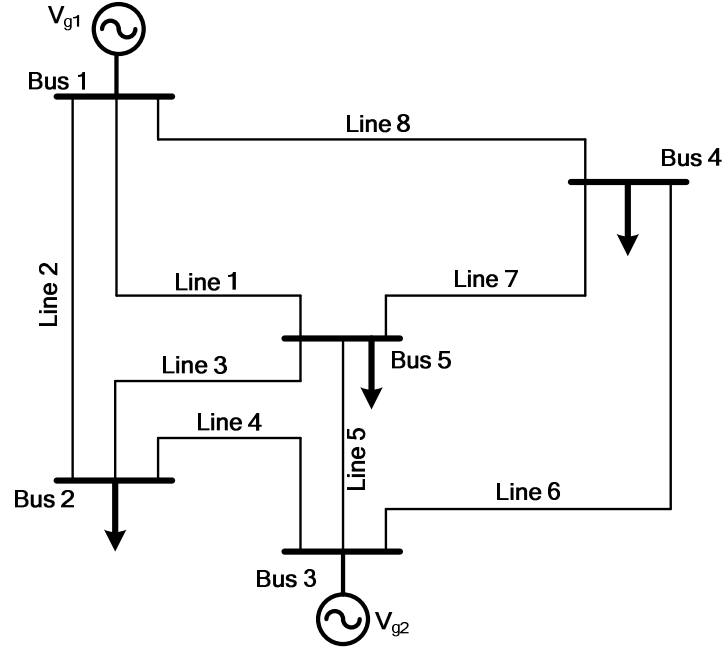


Figure 5.8: Example of a meshed network

Methods to control meshed networks are complex and usually require knowledge of the state of the system. In a meshed network with controllable elements such as LTCs, these states can be determined using off-line power flow simulations. The same off-line techniques can be applied to the CNT as the transformer can be controlled to achieve the desired final state of the system as determined using load flow studies.

An alternate approach would be to control the CNT using locally measured parameters. This is an extremely difficult problem as it is challenging to ensure minimal or no interaction occurs between multiple controllers in the network. The ability to control massively distributed assets autonomously based on locally measured information is possible and has been shown in [55]. The control strategy uses an exponential time constant that allows the system to gradually move toward the desired final state. The entire control scheme is implemented using locally measured parameters. A similar control strategy would be desirable for the CNT where local parameters such as node voltage and line current can be used to determine the set-point for operation of the transformer.

5.2.3.1 MODEL OF THE CNT

Control of the CNT is addressed by developing a model that represents the characteristics of the device. CNT behavior can be analyzed in the two-dimensional d-q plane. The DC component of the duty cycle, D in equation 5.3 controls the direct or d-component of the voltage V_d , which in turn regulates the magnitude of the output voltage of the transformer (in this case the bus voltage). The even harmonic component of the duty cycle controls the quadrature q-component of the voltage V_q . The quadrature component V_q determines the phase angle of the output voltage of the transformer. Using equation 5.2 the voltage at the output of the transformer can be split into V_d and V_q components as given by equation 5.6 and 5.7.

$$V_o = V_d + jV_q \quad (5.5)$$

$$V_d = V_m \left(-(1+N) \cdot K_0 + (1+N) + K_0 \cdot (1-N) \right) \quad (5.6)$$

$$V_q = V_m \left[\left(K_2 \cdot \frac{(1+N)}{2} \right) - \left(K_2 \cdot \frac{(1-N)}{2} \right) \right] \quad (5.7)$$

Here, V_o is the output voltage, V_q and V_d are the quadrature and direct components of the output voltage, V_m is the magnitude of the output voltage, and N is the turns ratio of the tap winding.

The model of the CNT considers power balance of the device. The CNT is a lossless device with power conserved at the fundamental frequency. There is however a dynamic exchange of energy between the third harmonic and the quadrature components. Using this knowledge an equivalent circuit model for the CNT is developed. The model of the CNT is shown in Figure 5.9, where I_d is the line current (which is also the current through the CNT).

The ability to control quadrature voltages at the fundamental frequency is represented by voltage sources V_d and V_q . V_d represents voltage magnitude control and V_q represents phase angle control. The power balance is achieved with a current source that represents the voltage in phase with the line voltage which provides the boosting function of the CNT.

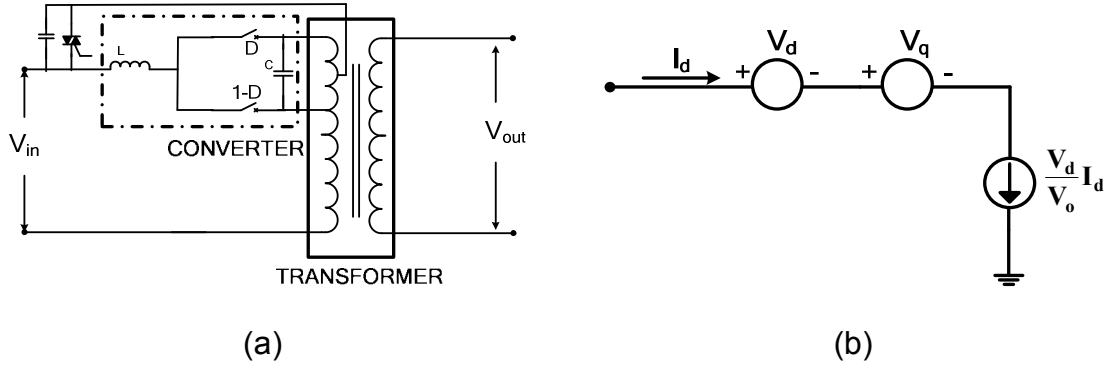


Figure 5.9: (a) CNT, (b) equivalent circuit

5.2.3.1 CONTROL OF CNTs

Control of multiple CNTs in a four-bus system is considered. The goal here is to test the model of the CNT in a complex system, with each device controlled autonomously.

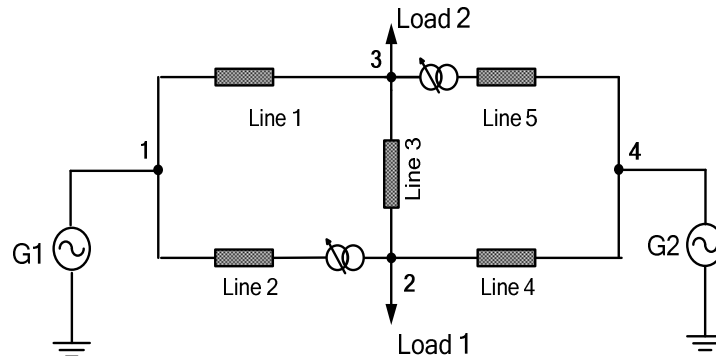


Figure 5.10: Schematic of four-bus system

The network has two generator buses and two load buses at a nominal voltage of 79 kV. Lines 2 and 5 are low impedance and thereby limit the maximum power that can be transferred through the network. The CNT is implemented at two nodes in the system. Each transformer is operated assuming knowledge of only local parameters, i.e., node voltage and branch current.

The approach used in controlling the transformers in a network follows the hierarchical control approach in any power system network. tier 1 is control of the bus voltage magnitudes between 0.95p.u and 1.05p.u. Tier 2 is control of the power flow in the network to ensure maximum utilization of the transfer capacity while satisfying constraints enforced by the thermal limits of the lines.

Figure 5.11 illustrates the drop in the bus voltages as the load on the system is varied. The plot shows bus voltages with and without the CNT control. In this example the CNT is designed to have $\pm 10\%$ control, and is installed on the load buses (bus 2 and bus 3).

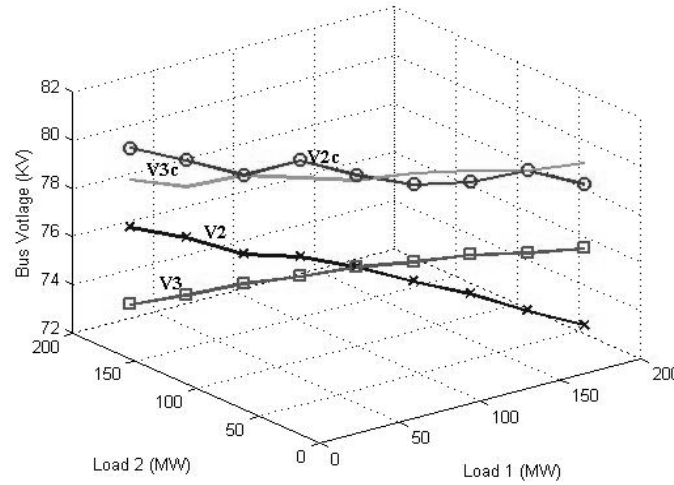


Figure 5.11: Variation of bus voltages with (V_{2c} , V_{3c}) and without (V_2 , V_3) CNTs

Control of power flow in the network using local parameters is achieved by controlling the phase angle of the output voltage of the CNT. The CNT has been controlled to emulate series impedance injection, i.e., the voltage synthesized by the CNT is in quadrature with the line current. The CNT can provide a fully controllable voltage in series with the line, similar to an SSSC.

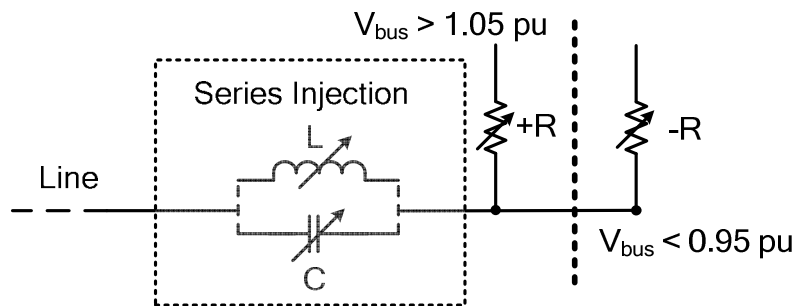


Figure 5.12: Model of the CNT using passive components

Figure 5.12 illustrates a simplified representation of the model of the CNT with autonomous control. The CNT control action is activated when the current

in the lines exceed the thermal limits. The current is then reduced by effectively increasing the inductance in the line by generating a voltage source in series with the line that leads the current by 90 degrees. The reverse can also be implemented, where the effective line reactance is decreased by generating a voltage source in series with the line that lags the current, thereby emulating a capacitor. Control of the bus voltages is achieved by either stepping up or stepping down the input voltage to ensure regulation. This is similar to using a positive or negative resistance that adds or subtracts in phase voltage.

The controlled line currents (line 2 and line 5) are shown in Figures 5.13(a) and 5.13(b). The control in this case is purely inductive, i.e., the voltage source injected by the CNT operation lags the line current.

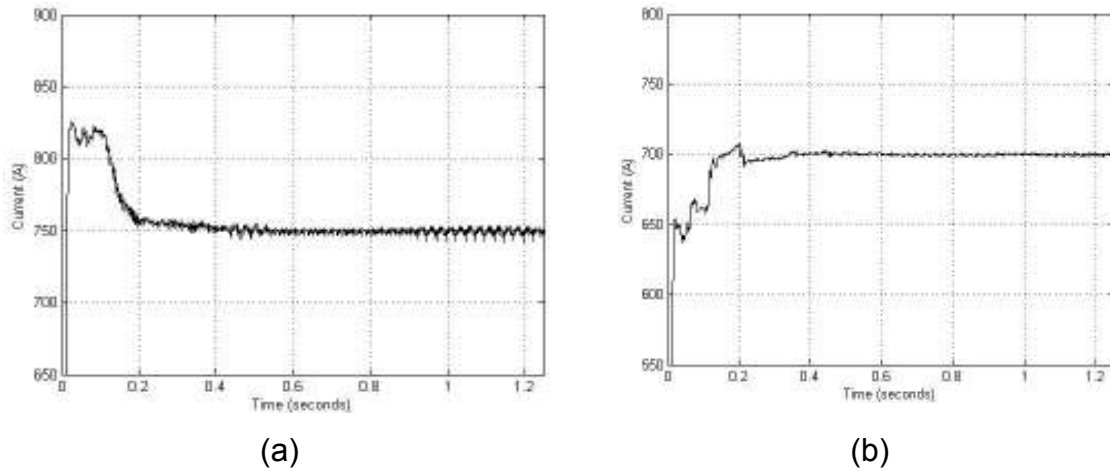


Figure 5.13: Line current (rms): (a) line 2, (b) line 5

Table 5.2: Line currents ($L_1 = 100$ MW $L_2 = 80$ MW)

Line	Line Current (A)	Thermal Limit	Regulated Current
1	498	750	534
2	853	750	750
3	95	750	99
4	260	700	346
5	650	700	700

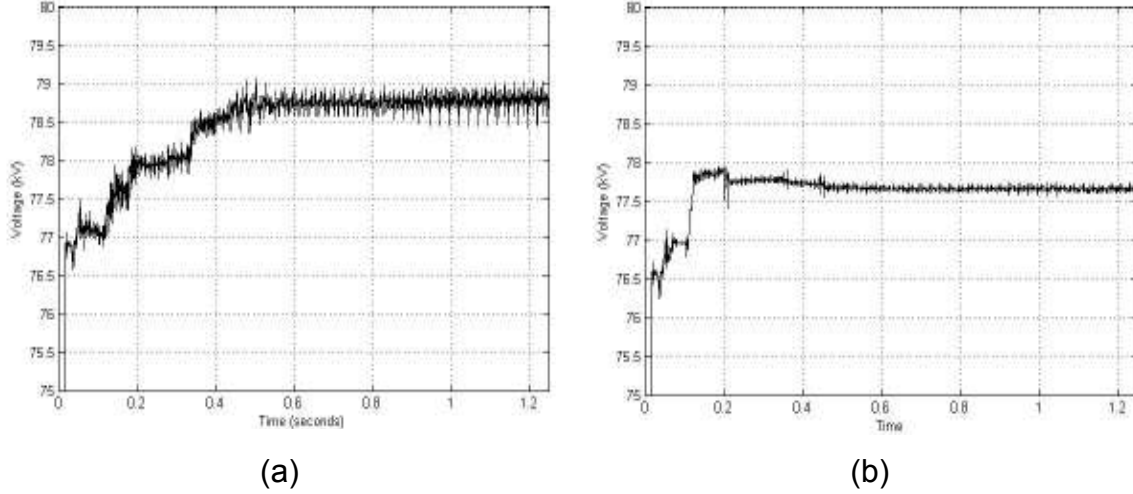


Figure 5.14: Bus voltage magnitudes (rms): (a) bus 2, (b) bus 3

The current in line 2 is controlled to 750 A and Line 5 to 700 A. The bus voltages are regulated between 0.98p.u and 1.02p.u. The regulated voltages are shown in Figure 5.14 (a) and (b). Table 5.2 details the line currents with and without CNT control.

5.2.4 TACC IMPLEMENTATION OF THE CONTROLLABLE NETWORK TRANSFORMER

The CNT is targeted for utility voltage and power levels. This implies that a cost effective converter needs to be designed and built to operate a distribution voltage levels to effectively realize this technology.

By way of example, the CNT used in the four-bus system has been rated with a $\pm 10\%$ tap at 79 kV. At nominal voltage the switches need to be rated to handle peak voltages of 22.35 kV. Commercially available semiconductor devices are not rated to handle these voltages. One method to realize these voltages is series connecting devices. This is challenging to implement and significantly increases the cost complexity of the system.

Realizing 22.35 kV peak voltages would require series connecting seven IGBTs rated at 6.6 kV, as shown in Figure 5.15. Devices rated at these operating voltages switch at frequencies in the range of hundreds of Hz which would degrade granularity of control of the device and increase filter requirements.

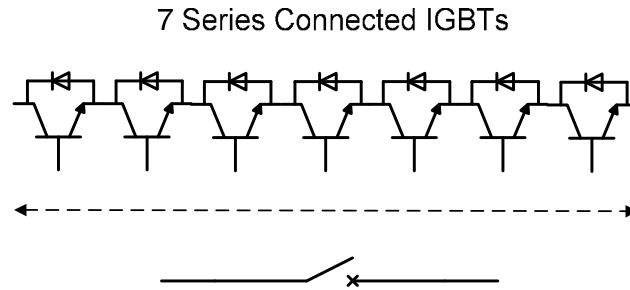


Figure 5.15: Series connected IGBTs to realize higher voltage levels

It is extremely important to address the issue of scalability of this technology to higher voltages and power levels. Multilevel direct AC converters, a novel approach to direct AC-AC power conversion provides a solution to scaling of this technology. The concept of multilevel direct AC converters will be presented in Chapter 6.

5.3 INVERTER-LESS ACTIVE FILTERS

All active filters today are based on DC-AC inverters with shunt type filters used to compensate for harmonic currents generated by non-linear loads. The load current is measured and the harmonic currents extracted, typically using a synchronous frame regulator [56], [57]. An error loop maintains DC bus voltage on the voltage source inverter. The combined feedback signal is transformed back into the stationary frame, and yields the reference currents for the inverter. The inverter then generates the harmonic currents that compensate for the harmonics in the load. Active filters generally provide well behaved harmonic compensation that is not susceptible to nearby capacitor banks and does not easily excite resonances.

Clearly, active filters today constitute a well understood and proven technology with a specific target application. Even then, the level of market penetration achieved by active filters continues to be small. One reason for this slow adoption is cost. The high device ratings required and the substantial energy storage needed results in high-cost and poor reliability. However, conventional wisdom dictates that active control of arbitrary harmonics requires a

voltage source inverter with PWM synthesis of the desired waveforms with the desired harmonics.

The application of the principle of virtual quadrature sources presents a unique approach to realizing active filters with no bulk energy storage, and without inverters. This results in a simple low-cost filter that provides harmonic compensation with no bulk energy storage.

5.3.1 INTRODUCTION TO ACTIVE FILTERS

It is important to understand some of the fundamental concepts associated with active filtering. At the most basic level, a shunt active filter draws desired harmonic currents from the line to compensate for harmonic currents generated by other loads or sources. Figure 5.16 shows a simplified schematic of an active filter. The input is a sinusoidal source voltage and the load generates harmonic currents that are to be absorbed by the active filter. Based on instantaneous power flow and the need to follow an arbitrary current waveform in an inductive filter element, it is widely believed that a four-quadrant power converter with energy storage is required to fulfill the desired control function. This is validated by a review of literature that shows that virtually all active filter topologies rely on an inverter, typically a voltage source inverter [58].

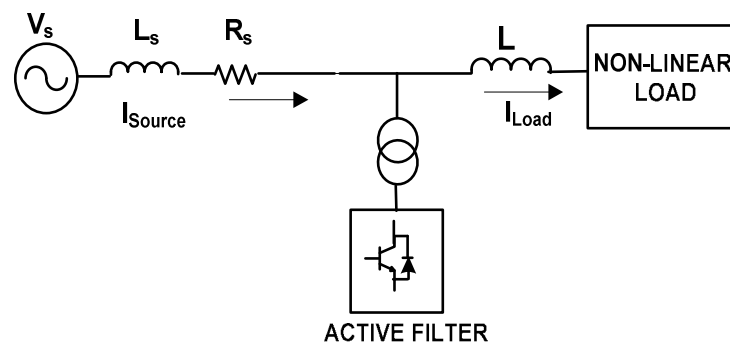


Figure 5.16: Schematic of typical active filter implementation

An alternate approach is possible, but is not widely used. This approach uses direct AC-AC matrix converters to synthesize active filtering functions. Minimal use of this topology for active filtering applications is primarily because the lack of independent energy storage per-phase in a matrix converter creates

direct coupling between low frequency components that flow in different phases. This makes it difficult, if not impossible to realize independent active filtering on the different phases, except under very limited specific conditions.

The proposed active filters are based on the novel concept of using the principle of VQS with a simple AC chopper. Three different sources of reactive and, or harmonic current are considered.

5.3.2 RESISTIVE INVERTER-LESS ACTIVE FILTERS (R-ILAF)

The VQS approach is seen to cause some very unusual characteristics in active filters. Possibly the simplest case is also the most unusual. It appears that it is possible to use a resistor with an AC switch and no energy storage to realize reactive and, or harmonic compensation. This device is called a resistive inverter-less active filter or R-ILAF. The very concept of realizing reactive or harmonic compensation with no reactive components or energy storage seems intuitively problematic as it requires operation of the filter in all four quadrants. Conventional thoughts suggest that a switch and resistor combination can provide only two-quadrant capability which is inadequate for effective harmonic compensation.

Even though the concept appears at first glance to be rather esoteric, it is likely that such functionality may actually have practical application. If one assumes that industrial plants frequently contain significant level of resistive loads, e.g., heaters, furnaces, and lighting.

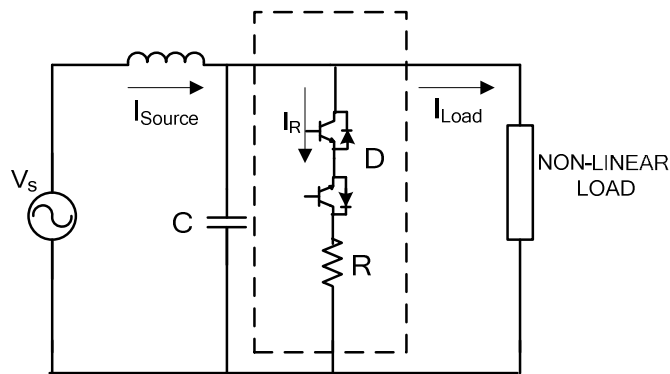


Figure 5.17: Resistive inverter-less active filter (R-ILAF)

The level of power delivered to the resistive load is normally controlled, often using a thyristor AC voltage regulator. However, the resistive load normally provides no additional functionality and the thyristor controller generates a high level of harmonics.

The ability to regulate the desired power to the resistive load while providing plant-level harmonic compensation can be achieved using the schematic shown in Figure 5.17.

A single AC switch in series with the resistor is used to regulate the effective duty cycle, and thus the power delivered to the load. A small low-pass LC filter is used to filter out switching harmonics. If the switch is operated with a constant duty cycle D at a constant frequency f , the power delivered to the load is given by,

$$P_0 = \frac{D^2 V_s^2}{R} \quad (5.8)$$

Where, P_0 is the power delivered to the load, V_s is the input voltage, and R is the resistance used in the active filter.

Regulating the power to the load can be achieved using simple duty cycle control. This mode of operation is consistent with AC choppers, and is well known [59].

Applying the principle of virtual quadrature sources, the following characteristics for the R-ILAF can be derived. Assuming the modulation signal to have only a DC and second harmonic component, the voltage across the load resistor is now seen to be given by,

$$V_R = D \cdot V_m \sin \omega t$$

$$D(\theta) = K_0 + K_2 \sin(2\theta + \varphi_2) \quad (5.9)$$

Where, V_m is the peak of the input voltage and V_R is the voltage across the resistor.

$$V_R = V_m K_0 \sin \theta + V_m \frac{K_2}{2} \cos(\theta + \varphi_2) - V_m \frac{K_2}{2} \cos(3\theta + \varphi_2) + \text{switching frequency components} \quad (5.10)$$

V_R consists of a fundamental component and a third harmonic with a controllable amplitude and phase. The power delivered to the load has spectral components at the fundamental frequency and associated harmonics, as well as at frequencies around multiples of the switching frequency of the AC switch. Computation of the power delivered to the load needs to take into account the various frequency components, but it is clear that as $D(\theta)$ is varied, the power delivered to the load can be smoothly controlled.

It is also important to observe that the line current drawn by the load is $i_R(t) = V_R(t)/R$. The amplitude of the third harmonic is controlled by the amplitude of the second harmonic component, $V_2 = V_m K_2/2$, and the phase of the third harmonic is dictated by the phase of the even harmonic, making the third harmonic current drawn by the resistor fully controllable. Similarly, if a fifth harmonic current is to be generated, it is necessary to add a 4th harmonic to the modulation signal $D(\theta)$. While this is seen to generate the desired fifth harmonic current to cancel the offending component, it also generates an additional third harmonic current. This third harmonic current now needs to be summed with the component generated by the second harmonic in $D(\theta)$ to realize the overall amplitude and phase desired for the third harmonic. It is clear that if harmonics are to be controlled to desired levels, one will be left with a quadrature component at the fundamental frequency that is not specifically controlled and may be undesirable. This discussion is also indicative of the overall control strategy that will need to be followed.

This argument can clearly be extended to additional frequencies. It should be noted that with the principle of virtual quadrature sources, a reactive source at the fundamental frequency is automatically induced, even though no such reactive components have been used. This again clearly shows that a resistor and switches can be used to emulate inductors, capacitors and active filters. The R-ILAF simulation results, shown in Figure 5.18 have a non-linear load generating a third and fifth harmonic, as well as a linear resistive load rated at 3.6 KW. The nonlinear load is simulated to inject 25% third harmonic and 10% fifth harmonic currents. This results in a load current with a total harmonic distortion

of 27%. As the harmonic currents are at the third and fifth harmonics, the modulation signal used has three components, the DC, second harmonic, and fourth harmonic components.

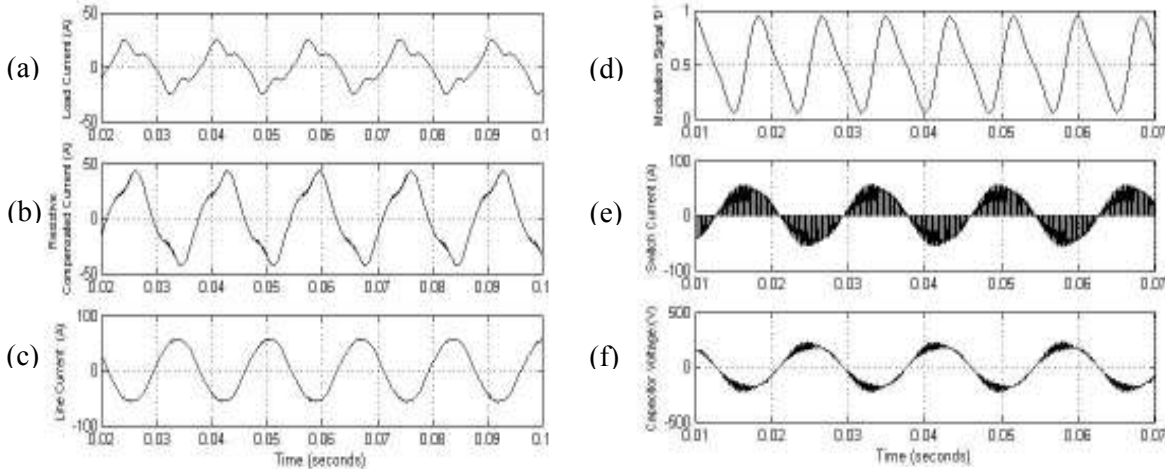


Figure 5.18: Simulation results for the R-ILAF. (a) load current , (b) resistive compensated current, (c) line current , (d) modulation signal, (e) switch current, (f) capacitor voltage

Figure 5.18 (a), (b) and (c) illustrate the load current, resistive compensated current, and the line current. The compensation of the harmonic currents has been achieved by controlling the AC switch to generate a current with harmonics in anti-phase with the load current. This results in a line current with THD of 4%. Figures 5.18 (d), (e) and (f) show the modulation signal, switch current and capacitor voltage.

The modulation signal has been chosen to minimize harmonics in the line current. The limitations on the ability to control the harmonics are set by the power delivered to the load, which has to be maintained constant; in this case the power is maintained at 3.6 KW. The FFT of the line and load currents is shown in Figure 5.19 (a) and (b). Through the action of the R-ILAF, the harmonics in the line current have been controlled to a minimum.

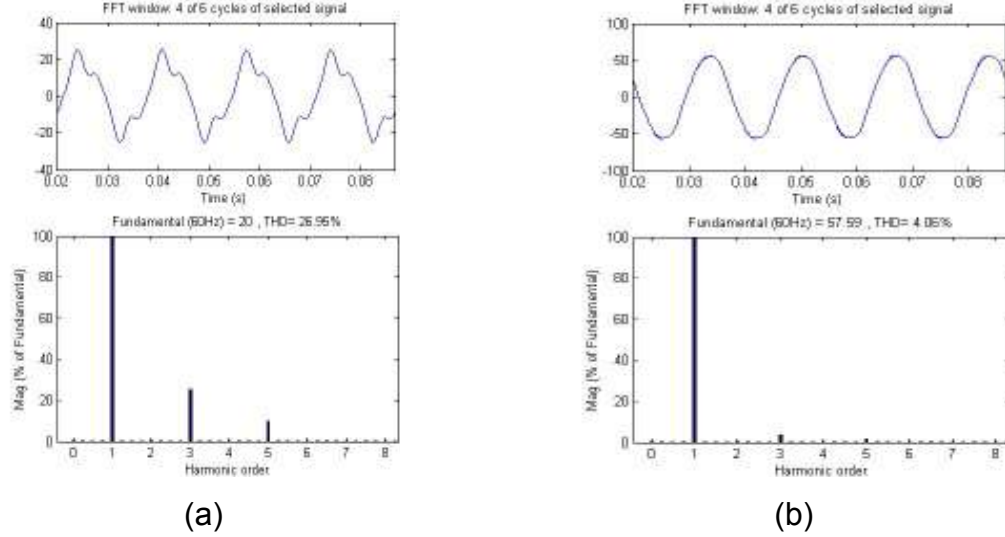


Figure 5.19: FFT (R-ILAF) (a) load Current with THD = 26.95%, (b) line current with THD 4.06%

Another method for implementing an R-ILAF includes an inductive filter for the resistor. This yields an LR-ILAF circuit. The switches are now controlled with a duty cycle D and $(1-D)$, where D is given by equation 5.9. This approach filters the switch voltage, V_{sw} , applying only the low frequency components to the resistive load. The power delivered to the load no longer contains the high frequency components, but is limited to the fundamental and harmonic frequency components only.

This may also prevent high dv/dt stresses being applied to the resistive loads, and will result in lower EMI and noise levels. As a result, the voltage across the load resistor can be seen to be:

$$V_R = V_m K_0 \sin \theta + V_m \frac{K_2}{2} \cos(\theta + \varphi_2) - V_m \frac{K_2}{2} \cos(3\theta + \varphi_2) \quad (5.11)$$

Where, V_m is the peak of the input voltage and V_R is the voltage across the resistor.

While the R-ILAF shows an intriguing possibility of realizing reactive and harmonic control with a resistor, it is unlikely that many realistic retrofit applications will exist, given the need to find an appropriately matched resistive load.

Of broader appeal is the question of integrating reactive and harmonic compensation requirements together. Use of capacitors and reactors for VAR compensation is widespread. The typical implementation is through the use of switched capacitors and a thyristor controlled reactor to realize a static VAR compensator (SVC). Often, the capacitors are paired with tuning reactors to realize a passive harmonic filter. Appropriate application of passive filters requires significant level of analysis of the site and the network, and is rarely used except for very large rated installations. It is therefore ideal to consider a single, low-cost device to realize both functions.

5.3.3 INDUCTOR INVERTER-LESS ACTIVE FILTERS (L-ILAF)

The concept of the Inverter-Less Active Filters can be extended to inductive (L-ILAF) and capacitive (C-ILAF) elements to be able to realize the benefits of dynamic VAR control with the ability to control characteristic harmonic currents. As such, this capability is reminiscent of a STATCOM, but does not require inverters or DC bulk energy storage, and can operate on a single-phase basis. Figure 5.20 shows the inductor version of the ILAF or L-ILAF.

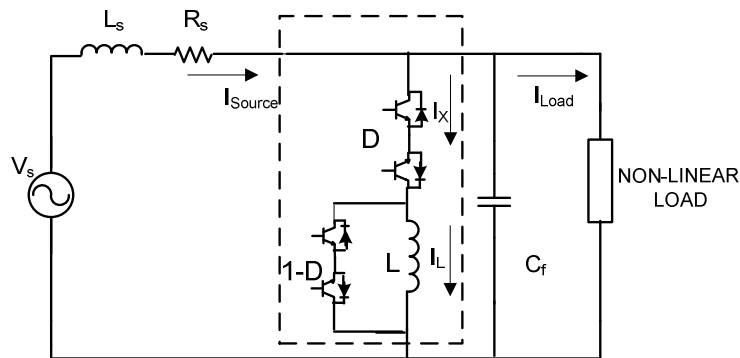


Figure 5.20: Schematic of inductor inverter-less active filter (L-ILAF)

As in the case of the R-ILAF circuit, the switches are modulated with a duty cycle $D(\theta)$ and $(1 - D(\theta))$. $D(\theta)$ contains a DC component (K_0), which represents the fundamental reactive VARs drawn by the ILAF circuit. For $K_0 = 1$, the maximum VARs are drawn, while for $K_0 = 0$, zero VARs are drawn. This principle is well known and understood.

Once again, the AC chopper duty cycle is modulated with even harmonic modulation.

$$D(\theta) = K_0 + K_2 s(2\theta + \varphi_2) + K_4 s(4\theta + \varphi_4) + \dots \quad (5.12)$$

The inductor voltage is then obtained by multiplying $D(\theta)$ with the line voltage. As in the case of the LR-ILAF, the inductor current can then be calculated and is seen to contain fundamental and third harmonic current.

$$I_L = \frac{-V_m K_0}{X_L} \cos \omega t + \frac{V_m K_2}{2X_L} \sin(\omega t + \varphi_2) - \frac{V_m K_0}{6X_L} \sin(3\omega t + \varphi_2) \quad (5.13)$$

The inductor current (I_L) is then reflected back to the line through the AC chopper switching function to provide the spectral composition of the line current (I_{LINE}) drawn by the AC chopper.

$$I_{Line} = \frac{-K_0^2 V_m}{X_L} \cos \omega t - \frac{K_0 K_2 V_m}{6X_L} \sin(3\omega t + \varphi_2) + \frac{K_2^2 V_m}{4X_L} \cos \omega t - \frac{K_0^2 V_m}{6X_L} \cos(3\omega t + 2\varphi_2) + \frac{K_2^2 V_m}{12X_L} \cos(5\omega t + 2\varphi_2) \quad (5.14)$$

Here, X_L is the inductive reactance of the L-ILAF at 60Hz.

If $D(\theta)$ is considered to be a constant DC term D , then the effective inductance seen by the line is $L_{eff} = D^2 L$. For the case where $D(\theta)$ includes the second EHM term, it is seen that I_L contains a third and a fifth harmonic, as well as the fundamental component. Similarly, addition of a fourth even harmonic component to the duty cycle will generate a fifth, seventh and ninth harmonic current.

Overall control of the ILAF involves tuning the levels and phase angles of the even harmonic modulation components to realize the desired harmonic current levels in I_L , and then tuning the DC component of the duty cycle to obtain the exact VARs required. It should be noted that the fundamental VARs and the level of harmonics all interact with each other. Figure 5.21 shows the simulation results for the L-ILAF, with the non-linear load consisting of 25% of third and 10% of the fifth harmonic currents.

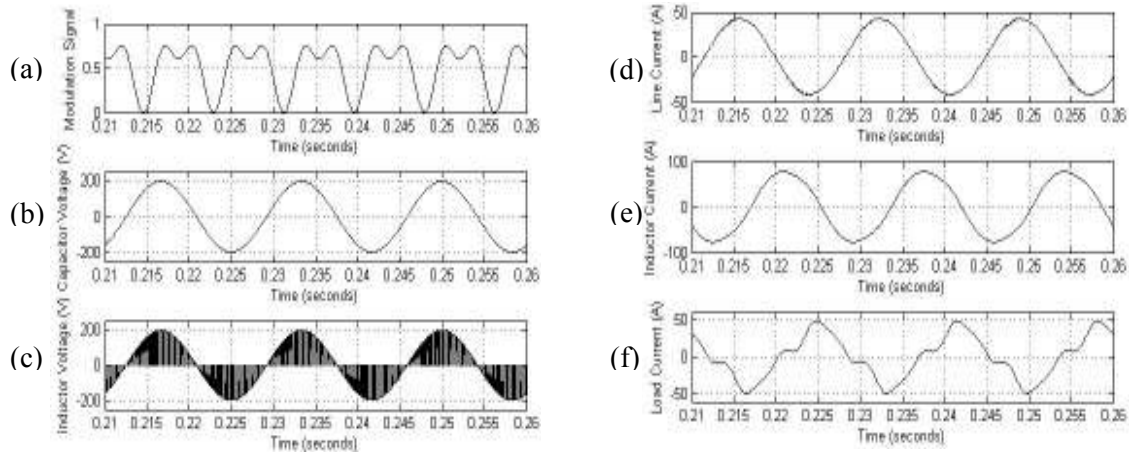


Figure 5.21: Simulation results for the L-ILAF. (a) modulation signal, (b) capacitor voltage, (c) inductor voltage, (d) line current, (e) inductor current, (f) load current

The line current, inductor current, and load current are shown in Figure 5.21 (d), (e), and (f) respectively. The inductor current in Fig 5.23(e) shows the distortion resulting from the even harmonics in the duty cycle. The modulation signal used to achieve the compensated harmonics shown in Figure 5.21(a). The modulation signal has both the second, as well as the fourth harmonic components. The magnitude and phase of both components have been determined to minimize harmonics in the line current.

For this particular example, the L-ILAF is controlled so as to draw 6 kVAR of reactive VARs at the fundamental frequency and compensate for the harmonics. The THD of the line current at the plant input drops to ~1%. The line current, with no harmonic content is illustrated in Figure 5.21(d).

The FFT of the line and load currents are shown in Figure 5.22 (a) and (b). These waveforms illustrate the ability to compensate for harmonics at multiple frequencies using the L-ILAF. The FFT of the line current shows a decrease in the overall THD from 25% to 1%.

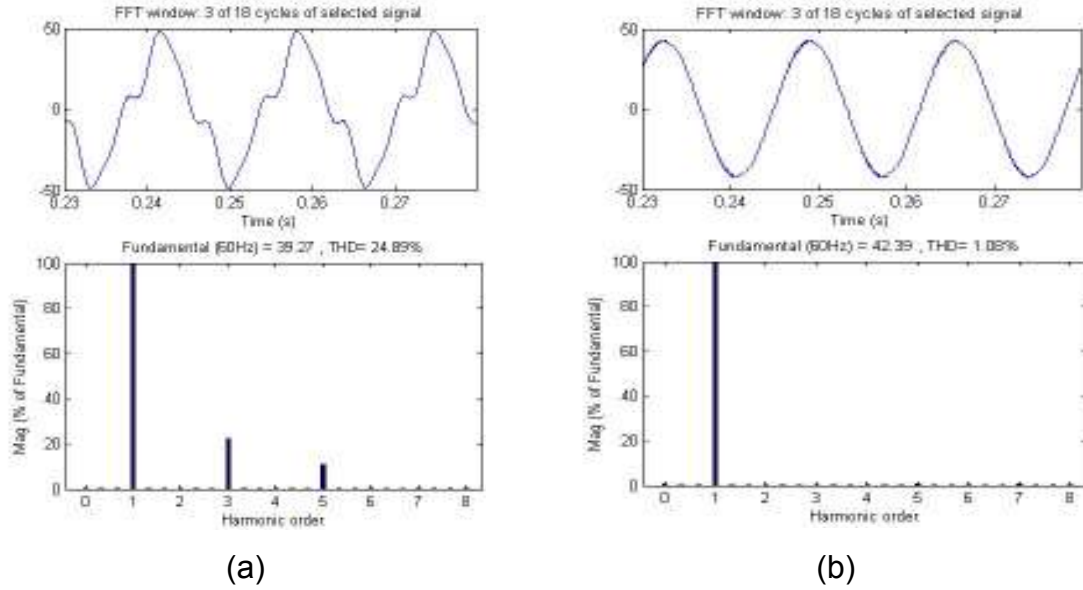


Figure 5.22: FFT (L-ILAF) (a) load current with THD = 24.89% , (b) line current with THD = 1.08%

The simulation results clearly demonstrate the ability of the L-ILAF to control VARs and harmonics. For the L-ILAF the range of control is fairly limited. This is because the harmonic currents in the inductor decrease with increasing frequency. Further, the harmonic voltages that can be created are a small fraction of the fundamental voltage. As a result, the range of control on harmonic currents is rather limited. It can be shown that with the L-ILAF, the maximum third harmonic current that can be drawn from the line is approximately 18% of the maximum reactive current that can be drawn. While this may be acceptable in many applications, it is important to see if a higher level of harmonic control is achievable.

5.3.4 CAPACITOR INVERTER-LESS ACTIVE FILTERS (C-ILAF)

By way of contrast, the capacitor-inverter-less active filter or C-ILAF has a much wider range of control. The C-ILAF shown in Figure 5.23 consists of two AC switches, a small filter inductor to filter out the high switching frequency content, and the main capacitor. The switches are operated with duty cycle D and $(1-D)$ as in the case of the L-ILAF. For the C-ILAF circuit, duty cycle

modulation is once again used at DC and even harmonic frequencies. Again, assuming only DC modulation with a duty cycle D , it is seen that the reactive current drawn from the line is $D^2 \cdot V_{rms} / X_C$, where X_C is the impedance of the capacitor at the line frequency.

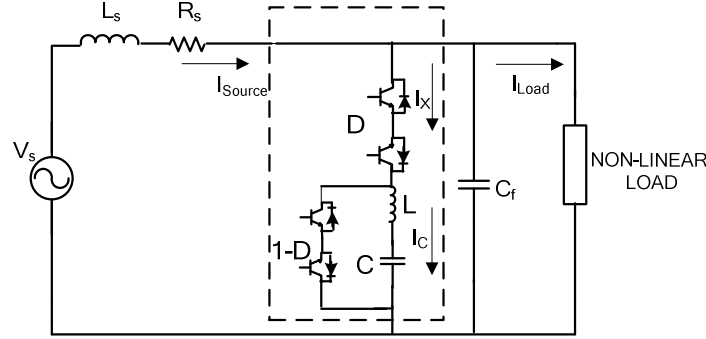


Figure 5.23: Schematic of capacitor inverter-less active filter (C-ILAF)

If modulation at the second harmonic frequency is considered, one sees that the third harmonic voltage impressed across the capacitor is

$$V_{C3} = \frac{-V_m K_2}{2X_C} \cos(3\omega t + \varphi_2) \quad (5.15)$$

This causes a third harmonic current in the capacitor given by,

$$I_{C3} = \frac{2K_0 K_2}{X_C} V_m \sin(3\omega t + \varphi_2) + \frac{K_2^2}{4X_C} V_m \cos(3\omega t + 2\varphi_2) \quad (5.16)$$

Here, X_C is the inductive reactance of the C-ILAF at 60Hz.

One can similarly calculate the fifth harmonic current that flows in the capacitor as a result of a fourth harmonic modulation component. It should be noted that while the harmonic voltage components generated are determined by K_2 and K_4 , the current increases with frequency as the impedance of the capacitor decreases. The effective current drawn from the line is once again calculated by considering the action of the switching function on the capacitor current. The fundamental component of the current and the fifth harmonic current in I_C , both result in a third harmonic current being drawn from the AC line. The magnitude of this third harmonic current is:

$$|I_{C3}| = \sqrt{4 K_0^2 K_2^2 + \frac{K_2^4}{16}} \quad (5.17)$$

When compared to the L-ILAF circuit, it is seen that the maximum third harmonic current that can be sourced to the line is approximately 51% of the maximum fundamental frequency capacitive current possible, three times as much as for the L-ILAF. Further, considering that most applications require leading VARs and harmonic control, the C-ILAF seems to be a very attractive and cost-effective implementation. Significant issues remain and need to be considered, the most important being the susceptibility to voltage spikes and transients.

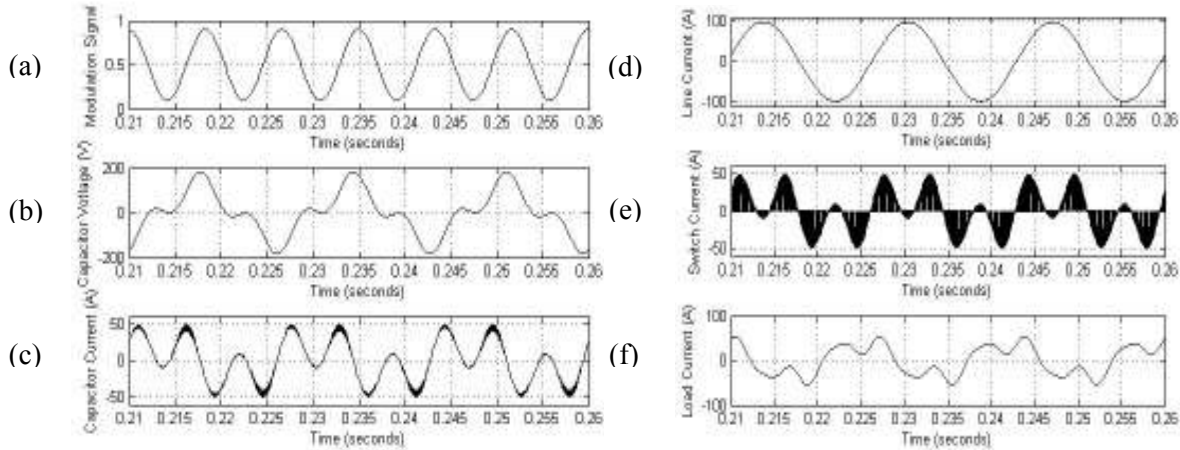


Figure 5.24: Simulation results for the C-ILAF. (a) modulation signal, (b) capacitor voltage, (c) capacitor current, (d) line current, (e) switch current, (f) load current

Figure 5.24 shows simulation results for a C-ILAF circuit operating with a single-phase non-linear load. Once again, it is seen that the harmonic levels can be reduced from a THD of 57.6% to as low as 1.67%, shown in Figure 5.25 (a) and (b). There are sufficient control handles to yield control of the fundamental frequency VARs, as well as multiple harmonic frequencies.

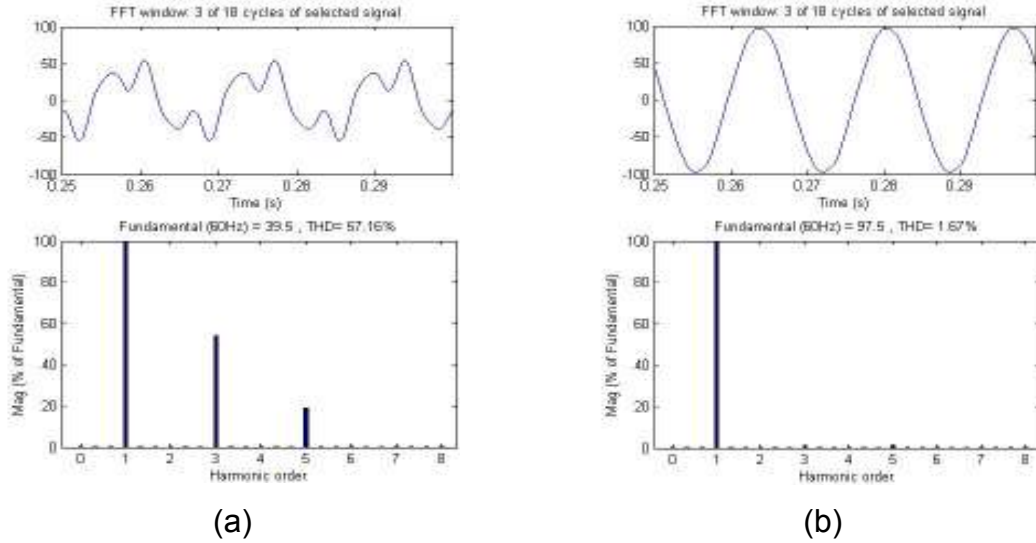


Figure 5.25: FFT (C-ILAF) (a) load current with THD = 57.6%, (b) line current with THD = 1.67%

Figure 5.26 shows the control range for fundamental VARs versus for harmonic compensation for the C-ILAF and I-LAF. The analysis assumes only a single harmonic is to be compensated. The range of control has been determined by varying the DC component of the modulation signal from 0 to 1.0 pu, and calculating the corresponding level of third harmonic current that is reflected into the line. The C-ILAF can be roughly seen to provide three times the level of harmonic current at the third harmonic as compared to the L-ILAF. The effect of phase of the second harmonic component of the modulation signal, ϕ_2 , has been illustrated for both the C-ILAF and L-ILAF. Three different values for ϕ_2 have been used to study the effect on the magnitude of the third harmonic components. The impact of ϕ_2 on the third harmonic component for both cases seems to be quite similar.

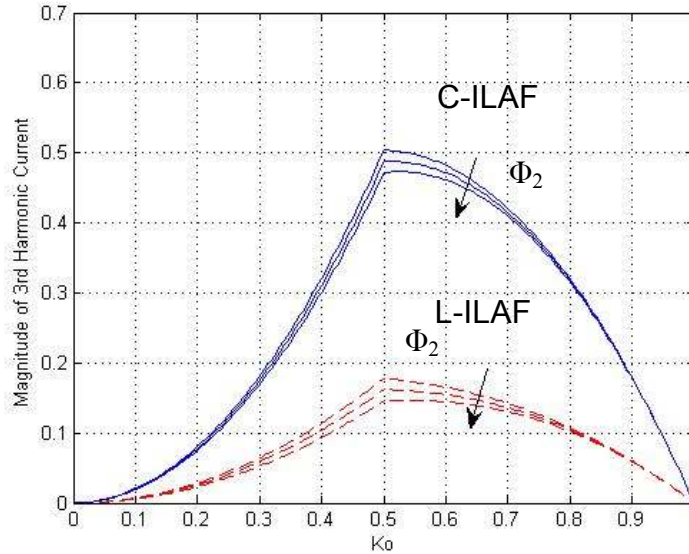


Figure 5.26: Control range for L-ILAF and C-ILAF

5.3.5 ILAF DESIGN CONSIDERATIONS

The design of ILAF circuits is quite different from that of typical active filters. Most active filters are designed with substantial energy storage. This allows the control of the system to be implemented in real-time, extracting a reference voltage or current that needs to be followed. Current regulators are then used to ensure that the desired waveform is followed within the bandwidth capability of the inverter and controller. All this presumes that the inverter has sufficient control headroom available, and uses a sufficiently small filter inductor to allow control action to minimize the existing instantaneous error. This causes the familiar trade-off between inverter switching frequency and losses, and the effective bandwidth over which the harmonic content can be minimized. The inverter itself uses electrolytic capacitors for energy storage. The electrolytic capacitor also necessitates protection during start-up, as well as under faults and transients.

Control of the ILAF circuits is based on creation of fundamental and harmonic frequency components that sum up to create zero-crossings that are coincident with the input line voltage. This allows synthesis of the desired voltage using simple duty cycle control. This in turn requires identification of

different harmonic components that satisfy the above constraints. In all cases of the ILAF, it has been seen that control of multiple objective functions, i.e. reactive and harmonic currents for the C-ILAF and L-ILAF, and control of power to the load and harmonic currents for the R-ILAF is possible.

Implementation of a controller that can operate in real-time is somewhat complicated. One approach is based on the establishment of multiple reference frames synchronous with the harmonic frequencies to be controlled. The highest harmonic frequency, say the fifth harmonic, is the component that is controlled first through the use of a fifth harmonic modulation in $D(\theta)$, using a PI controller to drive the component to zero. This then results in a third harmonic component being generated in the line current as a by-product. A second harmonic component is now added to $D(\theta)$, such that the third harmonic is also eliminated. This then causes a fundamental reactive component to be generated. Finally, the DC component of $D(\theta)$ is adjusted to realize the desired fundamental VARs or real power. It should be noted that this is an iterative process, as change in the DC component of $D(\theta)$ also causes change in the third and fifth harmonics.

It is also important to understand the ratings of the various components used in ILAF implementations. In a manner that is analogous to inverters, the concept of headroom can be defined and is seen to be very important. The VQS principle shows that maximum control of the quadrature components is realized at a DC duty cycle of $D = 0.5$. Thus, to achieve maximum control of harmonics, a simple method would be to define the nominal fundamental frequency operating point at $D = 0.5$. Some simple design examples are given below.

R-ILAF:

Specifications: 480 volts ac, 60 hertz, 1 MW resistive load (333 kW/phase) at $D=0.5$

ILAF Ratings: IGBTs – 2 X 1200V/400A, $I_{\text{harm max}} = 135$ Amps

C-ILAF:

Specifications: 480 volts ac, 60 hertz, 1 MVAR (333 kVAR/phase) at $D = 0.5$

ILAF Ratings: IGBTs – 4 X 1200V/400 Amps, $I_{\text{harm max}} = 200$ Amps.

By way of comparison, implementing the functionality of the C-ILAF system with STATCOM using voltage source inverters would require four IGBTs rated at 1200 V/400A, and an electrolytic capacitor rated at 800 volts. As there is no stored energy in the ILAF circuits, there are no soft-start or inrush current issues. The elimination of cross-coupling between phases and absence of stored energy also simplifies fault management, making the circuits more robust. These factors, along with a minimal component count significantly simplify system design and reduce cost. Device protection issues still need to be fully understood before an ILAF design can be scaled for high power operation.

5.3.6 EXPERIMENTAL RESULTS

Simple single-phase ILAF implementation has been done to validate the concept and to demonstrate that harmonic control can indeed be accomplished using simple AC choppers with no energy storage. Simple analog controls were used to synthesize the even harmonic, and manual tuning was used to achieve cancellation of the third harmonic load currents.

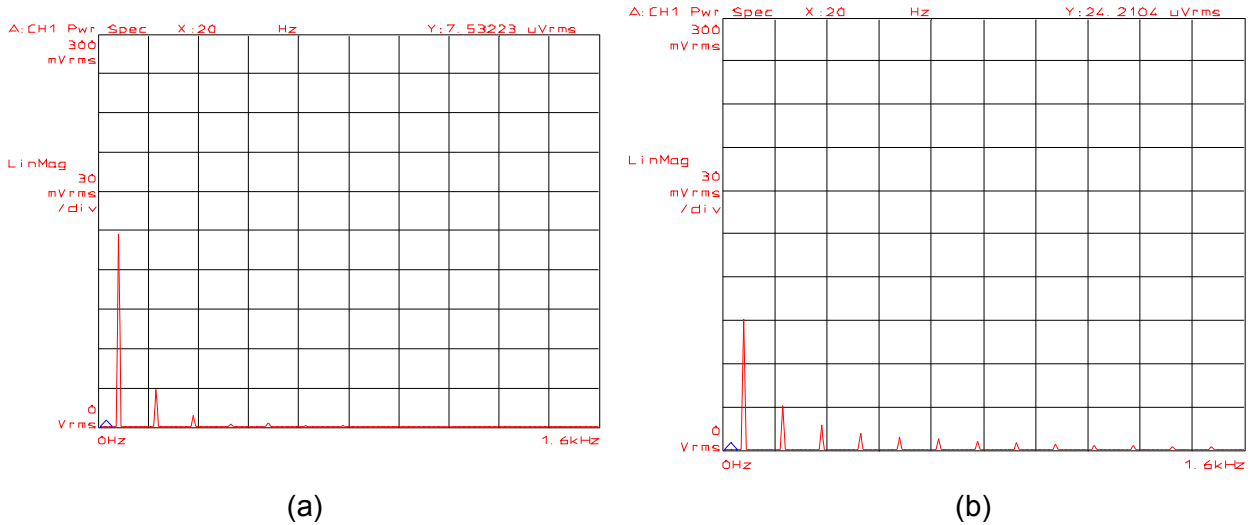
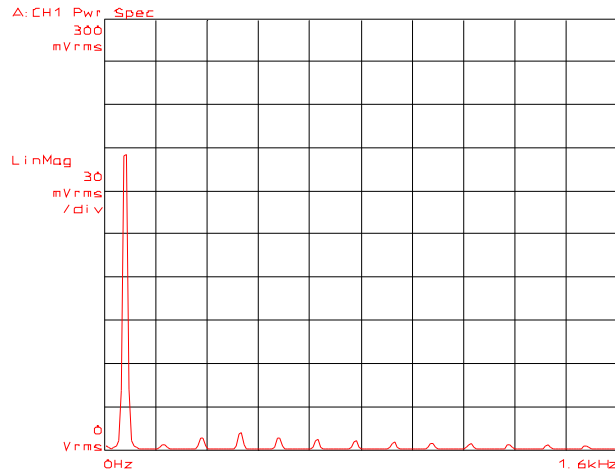
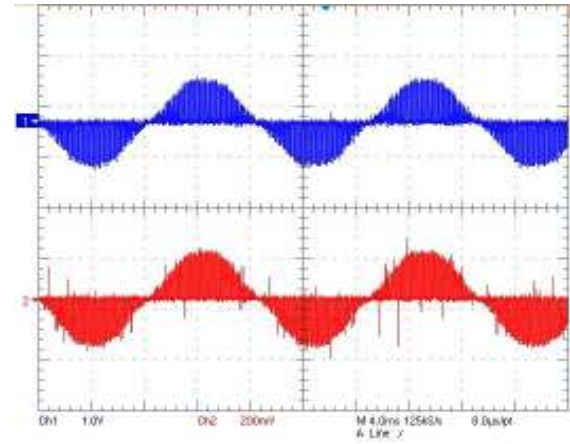


Figure 5.27: FFT (a) switch current, (b) non-linear load current,

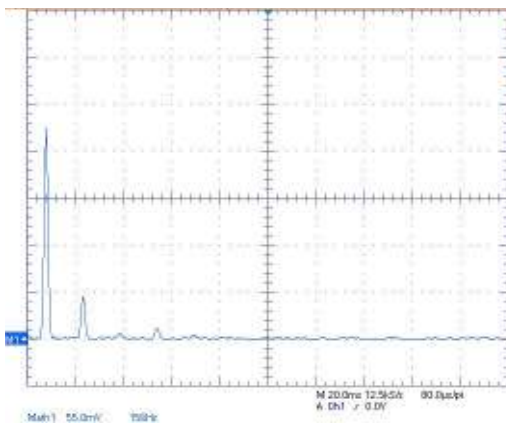


(a)

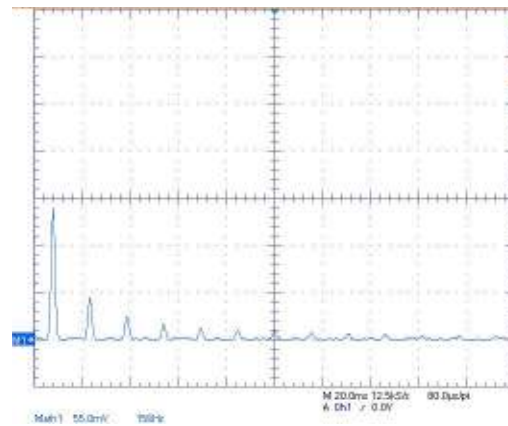


(b)

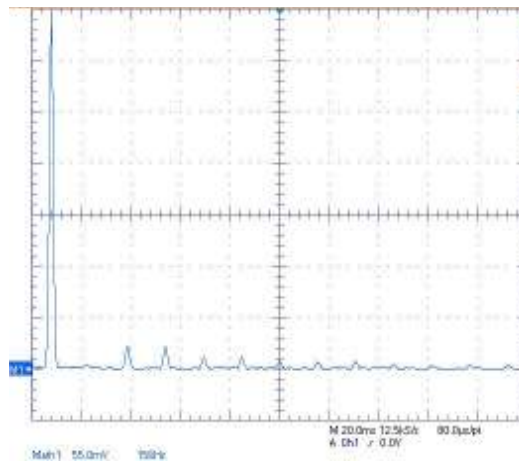
Figure 5.28: (a) FFT of the line current, (b) capacitor voltage, and voltage across 'R'.



(a)



(b)



(c)

Figure 5.29: FFT (a) switch current, (b) non-linear load current, (c) line current

Figure 5.27 and Figure 5.28 shows R-ILAF operation. The magnitudes of the fundamental and subsequent harmonics are illustrated. The harmonics of the non-linear load are generated using a single-phase rectifier. The third harmonic generated by the R-ILAF is tuned to cancel the third harmonic current generated by the rectifier load. Figure 5.28(a), illustrates the FFT of the source or line current which is free of the third harmonic.

Similar operation has been carried out for the C-ILAF. The experimental results obtained are illustrated in Figure 5.29. In this case, the third harmonics component has been compensated for.

5.4 CONCLUSIONS

Applications for the principle of virtual quadrature sources (VQS) have been presented in this chapter. The first application is the CNT. The CNT is a device that can be used in meshed power networks, that facilitates simultaneous control of voltage magnitude and phase angle to effectively regulate the power flow in the network while maintaining bus voltages within the required limits. The device is realized by augmenting an existing LTC with a TACC while applying the principle of VQS. The control capabilities of the CNT have been illustrated using a simple two bus system. A more complex problem of autonomous control of the multiple CNT's in a meshed four bus system has been studied. A simple model for the CNT has been developed to aid in the implementation of multiple devices in a network. Further, scaling of the CNT to realistic voltage and power levels has been briefly addressed.

Inverter-less active filters is a technology that controls reactive power and, or harmonic content of the currents in a system with no bulk energy storage. The different methods of achieving the same have been addressed using a resistive cell (R-ILAF), inductor cell (L-ILAF), and capacitor (C-ILAF). Simulation and experimental results have been presented to validate the control capabilities of these cells. Finally design examples for each type of active filter have been presented.

CHAPTER 6

MULTILEVEL DIRECT AC CONVERTERS

6.1 INTRODUCTION

Multilevel direct AC converters are a new approach to direct AC conversion that provides a solution to scaling to higher voltage and power levels. The multilevel converter is topologically similar to a flying capacitor inverter and can be used to synthesize an output voltage at the same frequency as the input, i.e., it is a non-frequency changing converter. This converter has been proposed to realize augmented functionality of existing grid assets such as shunt VAR capacitors [54] and LTCs [52]. This concept has been discussed in detail in Chapter 4.

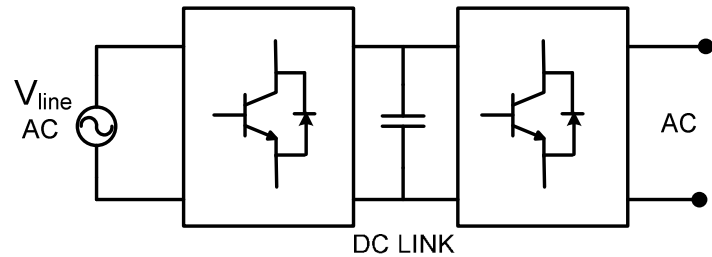
The multilevel direct AC converter presented in this chapter has characteristics that are desirable in power converters for utility applications. Properties such as the fail-normal mode and no bulk energy storage elements are some important advantages of the converter. Challenges with scaling to higher voltage and power levels will be addressed in this chapter.

6.2 DIRECT AC-AC CONVERTERS

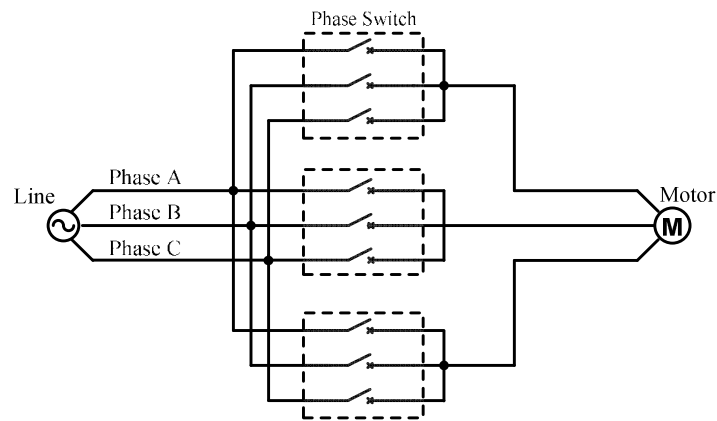
There are two characteristics that a direct ac-ac power converter for utility applications should have. First, the converter should provide power line conditioning with a minimalist topology while keeping size and cost low. The converter should also be scalable to utility voltage and power levels and have high reliability. Meeting both these criteria is crucial and non-trivial.

Conventionally direct AC-AC power conversion is achieved using one of two approaches. The first approach uses back-to-back voltage sourced converters (BTB VSC's) as shown in Figure 6.1(a); the second uses a matrix converter. An important advantage of the back-to-back converter is the ability to fully control the

output voltage of the converter. This is because the converter has a bulk energy storage element in the form of the DC link capacitor that provides the required energy to synthesize any phase angle and harmonic component.



(a)



(b)

Figure 6.1: Methods of AC line conditioning (a) back to back converter, (b) matrix converter

The matrix converter provides the same level of control as the BTB converter. In the matrix converter energy to synthesize a fully controllable output voltage is obtained from the multiple AC sources at the input. These sources are effectively energy storage for the converter.

Complexity and cost are both factors that have impeded widespread use of these technologies. Cost associated with bulk energy storage in the case of BTB converters, and complexities due to cross-coupling between phases in a matrix converter are some noteworthy drawbacks.

The direct AC-AC converter discussed in this chapter is a minimalist converter that provides direct AC-AC power conversion with no bulk energy

storage. The converter is similar to a flying capacitor inverter and is scalable to realistic utility voltage and power levels. Figure 6.2(a) shows the simplest form of a direct AC converter, i.e., the AC chopper. The proposed multilevel converter is shown in Figure 6.2(b). Although many multilevel DC-AC inverter topologies are known, extending them to direct AC operation has proved challenging.

The converter consists of cells that can be cascaded to realize a multilevel converter. The modes of operation and methods of control will be discussed in this chapter. The 3-level converter shown in Figure 6.2(b) comprises of four AC switches and small filter components C_{f1} , C_{f2} and L_f .

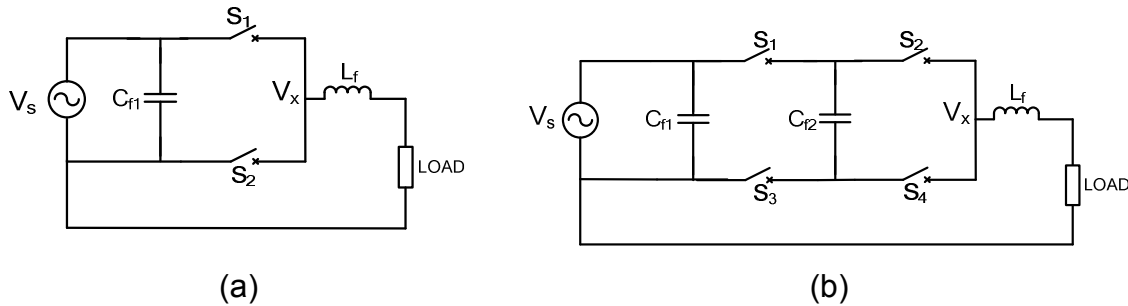


Figure 6.2: Direct AC-AC converter, (a) 2-level AC chopper, (b) 3-level

6.3 MULTILEVEL DIRECT AC CONVERTERS – AN INTRODUCTION

While the possibility of realizing TACCs with a simple AC chopper has been shown, a big question remains – how can this be scaled to higher power levels?

Challenges faced when operating at high voltage and power levels are because of the high voltage and current stresses that the semiconductor devices are required to handle. Commercially available 1700, 400A IGBT's that are low-cost and available in large volumes are ideal for industrial applications for operation at 480V. These devices operate with relatively high switching frequencies (tens's of kHz). An ideal scenario would be to use these low cost devices at voltage levels in the range of 4.16 kV – 13.8 kV. Series connecting IGBTs is one possible method to achieve this. As an example operating at 4.16 kV would require series connection of seven 1700V IGBTs. This method is complex because of problems associated with static and dynamic voltage sharing of series connected IGBT's [60], [61]. Also, reliability becomes a

problem as failure of a single device affects could result in the inability to operate the entire string of devices. Realizing these voltages with high power devices is also possible. For the same voltage, 4.16 kV, two series connected 6 kV IGBT's would be needed. There are however other issues with high voltage devices that include low switching frequencies (hundreds of Hz) due to long tail times and high-cost.

Consider the chopper cell shown in Figure 6.3(a) where the operating voltage of the converter is V . The addition of a second cell scales the operating voltage to $2V$. A converter with N blocks or cells would operate with a voltage of NxV . It is assumed that each cell or block has an effective voltage between the input and output of V . This maintains device voltage ratings at V while enabling converter operation at NxV . For example, a 4-cell or 5-level converter with 3.3 kV IGBTs can be operated at 4.16 kV. (The converter has four cells and five levels of voltages between which it can be switched, hence 4-cell or 5-level).

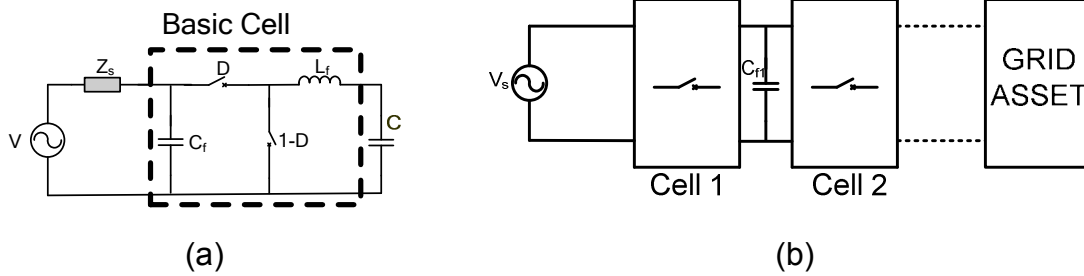
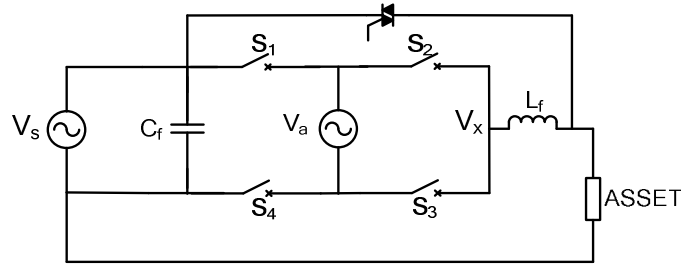


Figure 6.3: (a) buck AC chopper, (b) cascaded structure of multilevel direct ac converter

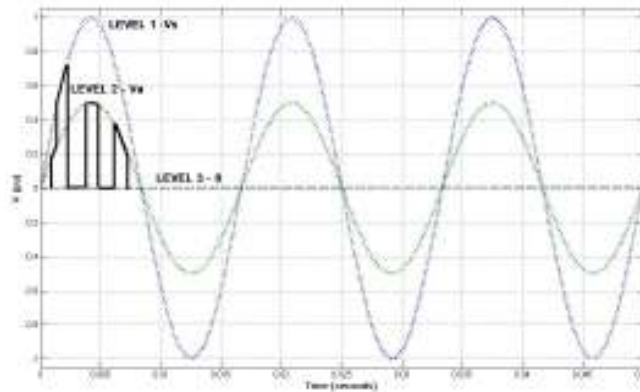
Consider the the 2-cell converter shown in Figure 6.4(a). This is the simplest form of the multilevel direct AC buck converter. The 3-level (2-cell) direct AC converter consists of switches $S1-S4$, small filter components L_f and C_f , and an auxiliary source V_a . The switch $T1$ is included in the 3-level direct AC converter to enable the fail-normal mode of operation.

Switches $S1$ to $S4$ are bidirectional gate turn-off switches that can be realized with two series connected IGBTs or other well known devices [62]. The voltage V_s is the sinusoidal line voltage. The auxiliary voltage V_a in this case, is $V_s/2$ and is also assumed to be sinusoidal. The AC converter has three voltage levels to switch between V_s , $V_a = V_s/2$ and 0 . The converter output voltage V_x ,

prior to filtering, can take on three distinct levels 0, $V_s/2$, and V_s . The converter is a buck converter as the output voltage at any instant of time is less than or equal to V_s .



(a)



(b)

Figure 6.4: 3-level direct AC converter (a) buck converter (b) available voltage levels

The available voltage levels are used to synthesize the desired output voltage by using the different switch states. Each of the allowed switching states generates a specific voltage on the output. The voltage levels for the 3-level or 2-cell converter are shown in Figure 6.4(b).

This idea extends to additional levels, where the synthesized output voltage is a result of the available voltage levels. Figure 6.5 illustrates the available voltage levels for a three, four and five level direct AC converter.

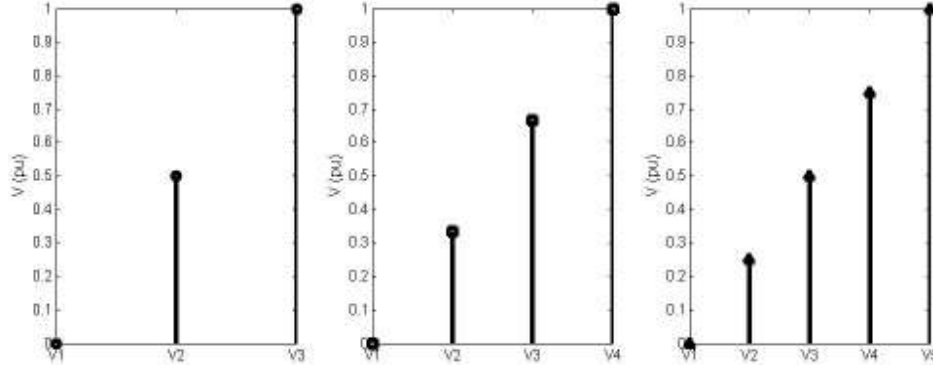


Figure 6.5: Voltage levels in a three, four and five level direct AC converter

As the number of levels increase the output voltage is synthesized with smaller steps allowing for operation of the converter at lower switching frequencies, lower peak voltage stresses across the devices, and lower filter requirements on the output. Steps in the voltages are given by:

$$V_k = \frac{(k-1) \cdot V_s}{n-1} \quad k = 1, 2, \dots, n \quad (6.1)$$

Where, n is the number of voltage levels for the converter and V_s is the voltage at the input to the converter.

6.3.1 MODES OF OPERATION OF A 3-LEVEL DIRECT AC CONVERTER

The 3-level direct AC converter has four modes of operation. V_x is the pre-filtered voltage at the output, V_a is the midpoint voltage and V_s is the voltage at the input to the converter. The modes of operation are shown in Figure 6.6. When switches S1 and S2 are ON the converter operates in mode 1 where, $V_x = V_s$. Mode 4 occurs when S3 and S4 are ON, where $V_x = 0$. Finally when switches S1 and S4 or S2 and S3 ON, the output voltage is $V_x = V_a = V_s/2$ (mode 2 and mode 3 respectively).

Switches S1 and S3 or S2 and S4 cannot be turned on together as that would result in shorting of one of the two voltage sources.

Table 6.1: Modes of operation for a 3-level buck converter

	S1	S2	S3	S4	V_x
MODE 1	ON	ON			V_s

MODE 2	ON		ON		$V_s/2$
MODE 3		ON		ON	$V_s/2$
MODE 4			ON	ON	0

The desired output voltage is therefore synthesized using a combination of the 4 modes of operation. This voltage is filtered by the output filter (including L_f) to give the desired output voltage and current. The maximum voltage stress across each switch is seen to be limited to the peak value of $V_a = V_s/2$, even though an output voltage of V_s can be realized.

The 3-level converter configured as shown in Figure 6.6(a)-(d) behaves like a buck converter, i.e., the voltage can be stepped down to a value between 0 and V_s by controlling the duty cycle D given by:

$$D = d1 + d2 + d3 + d4 \quad (6.2)$$

Where $d1$, $d2$, $d3$, and $d4$ are the ratios of the time spent in each mode (M1-M4) to the total time of each switching cycle.

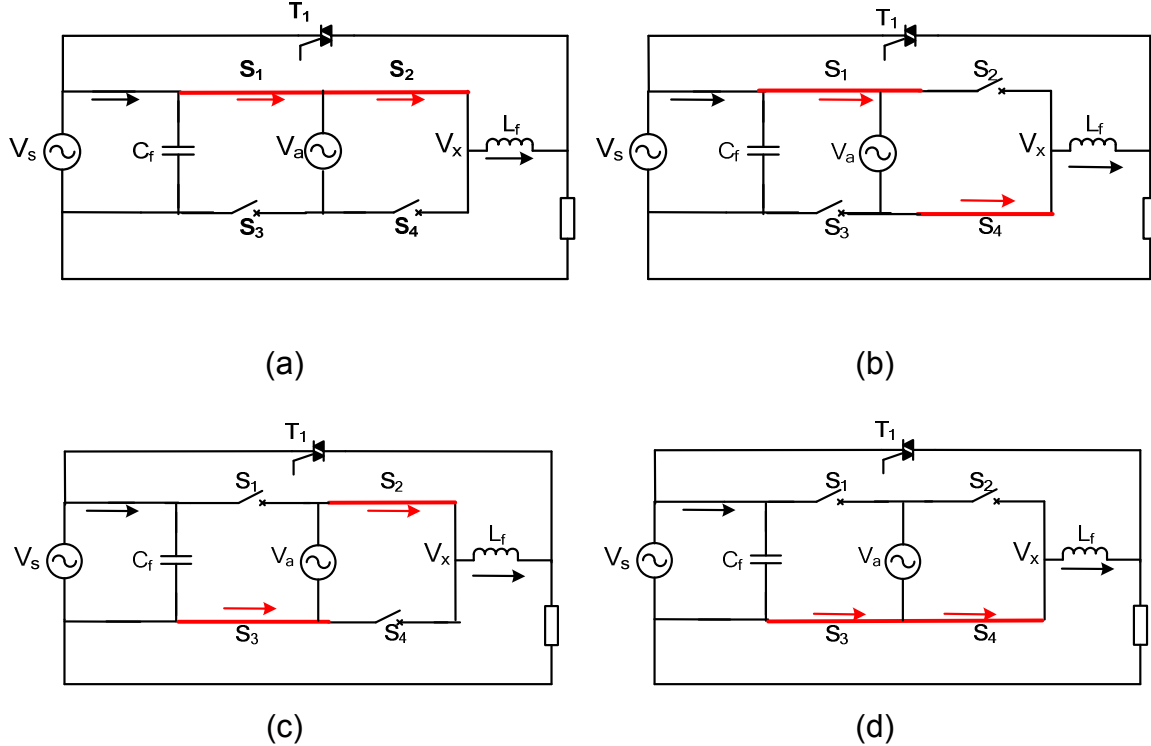


Figure 6.6 Modes of operation, (a) model 1, (b) mode 2, (c) mode 3 and (d) mode 4

The output voltage V_x can then be expressed as,

$$V_X = d1 \cdot V_S + d2 \cdot V_a + d3 \cdot V_a + d4 \cdot 0 \quad (6.3)$$

A 3-level boost converter can be realized by swapping the load and the source. The modes of operation for the boost converter remain the same, as described for the buck.

It is important to understand how the current I_o flows through the various switches in the four allowed states. In mode 1 and mode 4, there is no current flowing in V_a , as the voltage V_s is directly connected to the load circuit. In mode 2, the current $I_a = I_o$, while in mode 3 $I_a = -I_o$. The output voltage in both states is still $V_s/2$. This suggests that if a capacitor were used to realize V_a the capacitor charge could be maintained by having equal amounts of time spent between modes 2 and 3. However, as the voltage is not constant (as in a DC-AC inverter), but needs to vary sinusoidally, a complex control method would be required to control the voltage V_a . As the capacitor can be completely charge balanced every cycle, it suggests that only a relatively small capacitance would be required to maintain the voltage ripple of over one switching cycle at relatively modest levels. Further discussion on methods of control of the voltage is presented in Section 6.4.1.

6.3.2 FOUR-LEVEL DIRECT AC CONVERTER

To illustrate scalability of this converter the multilevel converter discussed in Section 6.3.1 is extended to a 4-level direct AC converter shown in Figure 6.7.

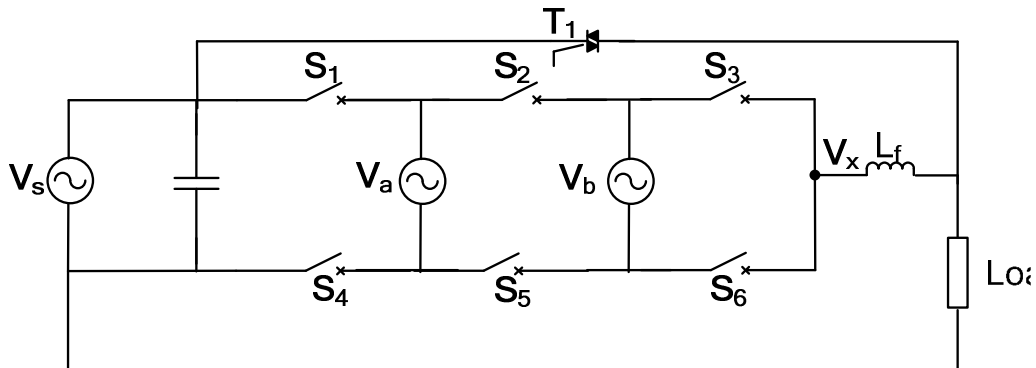


Figure 6.7: 4-level direct AC converter

The four-level converter uses six ac switches (realized using twelve IGBTs), and two voltage sources V_a and V_b , to synthesize a voltage V_x on the output. This voltage can be fully controlled between V_s and zero volts. The intermediary voltage sources are controlled so that $V_b = V_s/3$ and $V_a = 2V_s/3$.

Table 6.2: States and capacitor charging for the 4-level AC converter

State	Switches	V_x	Current in V_a	Current in V_b
1	S1S2S3	V_s	0	0
2	S1S2S6	$2V_s/3$	0	+ i_o
3	S2S3S4	$2V_s/3$	- i_o	0
4	S3S4S5	$V_s/3$	0	- i_o
5	S1S5S6	$V_s/3$	+ i_o	0
6	S2S4S6	$V_s/3$	- i_o	+ i_o
7	S1S3S5	$V_s/3$	+ i_o	- i_o
8	S4S5S6	0	0	0

Normal operation of the converter requires three AC switches to be in the ON state at any given time. Further, the switch pairs S1S4, S2S5 and S3S6, may never be turned on together, as it would result in the short circuit of a capacitor or a voltage source. This then leaves eight allowable distinct states that can synthesize four distinct voltages at V_x . Table 6.2 summarizes the details.

By way of example, implementation of the 4-level direct AC converter with low voltage IGBTs result in 12x1700 volt/1000A IGBTs for a power level of 1.44 MVA/phase at 2.4 kv volts line-neutral (4 kV volts line-line).

It is clear that the number of levels can be increased as needed to scale the converter for even higher voltage levels. It is possible to use higher voltage IGBTs or GTO devices to scale to higher voltage levels. This would of course require that the devices switch at lower frequencies.

Finally, the availability of new device technologies, such as SiC gate turn-off devices rated at 10-20 kV, may allow extension of this technology to medium and high voltage applications up to 230 kV.

6.4 DESIGN AND IMPLEMENTATION ISSUES

Design and implementation of the direct AC converter will be addressed in this section. There are challenges associated with the design and robust operation of the converter. Scaling of the direct AC converter is possible using the cascaded structure discussed in the previous section. It is however important to mention that the converter operation discussed so far assumes available voltage levels to switch between to simultaneously maintain device stresses and control the output voltage to the desired level. Clearly having controlled voltage levels to switch between is crucial for operation of the converter, as failure to do so will result in the failure of the devices because of increased voltage stresses.

6.4.1 CONTROL OF MULTILEVEL DIRECT AC CONVERTERS

The multilevel direct AC converter presented so far has been shown to be similar in structure to the flying capacitor inverter. The advantages that are seen topologically in scaling to high voltages using flying capacitor inverters are accompanied with complex control and loss of control range because of challenges with balancing the flying capacitor voltages. This makes the topology less attractive. Most approaches that address the balancing of these voltages use modulation strategies to achieve this [64], [65]. In addition to regulating voltage levels to the desired value, voltage ripple of the DC bus needs to be maintained at an acceptable value. This implies an increase in the size of the flying capacitors.

The multilevel direct AC converter is quite different from a control standpoint. While the requirements are the same i.e. regulating voltages across the flying or snubber capacitors, the methods are significantly different. A detailed look at three different control methods will be presented in the following section. The control methods are:

1. Control using capacitor charge balance
2. Control using a small-rated transformer
3. State-based control

6.4.1.1 CONTROL USING CAPACITOR CHARGE BALANCE

The first method for controlling the intermediary voltages in a multilevel direct AC converter is using switch modulation to provide charge balance of the capacitor.

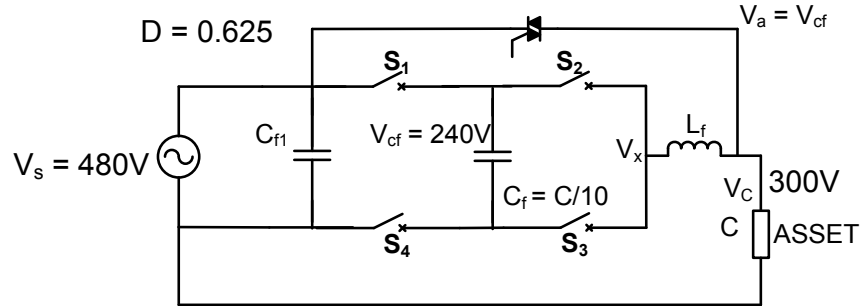


Figure 6.8: 3-level direct AC converter

The control method is explained using a 3-level direct AC converter. The 3-level converter shown in Figure 6.8 is operated with an input voltage $V_s = 480\text{Vrms}$. Assuming the output voltage needs to be regulated to $V_o = 300\text{V}$, the capacitor voltage V_{cf} would need to be controlled to 240Vrms so as to maintain voltage stresses across each ac switch at half of the input voltage. The filter capacitor C_f is assumed to be 1/10th of the output capacitor C as it is a snubber capacitor and does not need to be large. The modes of operation of the converter are as shown in Figure 6.6(a) to (d).

Table 6.3: Modes of operation for the 3-level AC converter

Mode 1	charge C
Mode 3	charge C_f
Mode 3	discharge C_f
Mode 4	freewheeling mode

Regulating the capacitor voltage V_{cf} is achieved by using the control structure shown in Figure 6.9. During every switching cycle the voltage across C_f is sensed and the error ΔV is used to determine the ΔQ and corresponding Δt

needed to increase or decrease the voltage across the capacitor. An assumption made in this method is that I_0 is constant during a single switching cycle.

The limits on the time spent in modes 2 and 3 to charge and discharge the capacitor is $0 - (1-D)t$. The time spent in mode 2 or 3 is given by equation 6.4.

$$\Delta t = \frac{I_0 \Delta V}{C_f} \quad (6.4)$$

Where, I_0 is the load current, ΔV is the instantaneous error in the capacitor voltage, Δt is the time required per switching cycle to control V_{cf} , and t is the switching period.

Based on the difference between the current state and desired state, an appropriate mode of operation is selected, using Table 6.3.

Controlling the voltage to the desired value using this technique at first glance seems fairly simple. At every switching cycle the required ΔV is determined and the corresponding charge required is either dumped into or removed from the capacitor. In principle this would result in a controllable AC voltage across C_f . There are however fundamental issues with this method that could lead to unstable and undesirable operation of the converter.

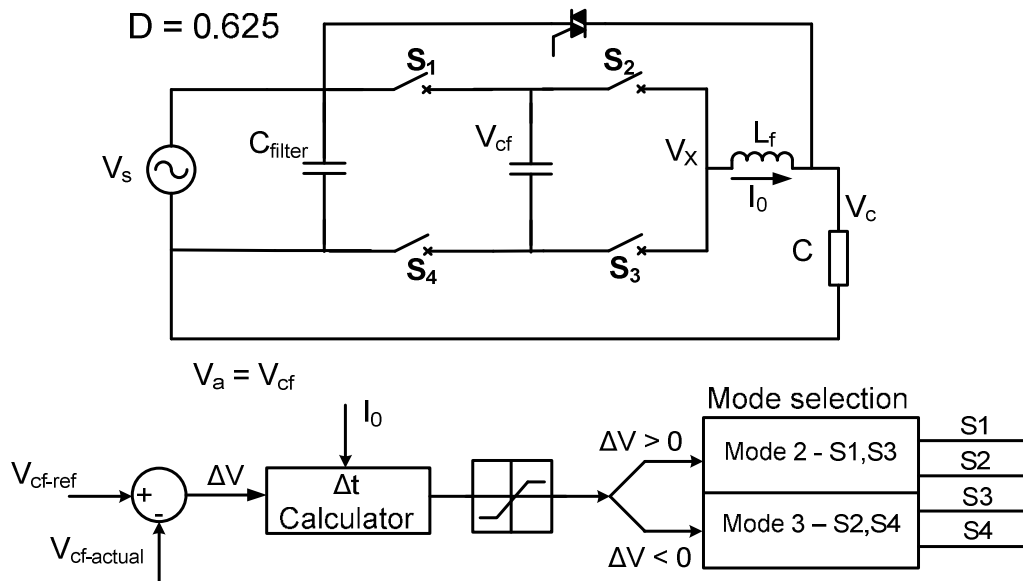


Figure 6.9: Control scheme for 3-level direct AC converter

The first is the complexity of control. If the converter in question is always a 3-level converter, implementation of the control method is not an issue. However, as the number of levels is increased the control loop for each level would need to operate independently within the available control region. The control region is determined by the operating conditions and desired output voltage. This would mean that in every switching cycle the amount of time available for charge balancing of the capacitor is equal to $(1-D)/f$, where, f is the switching frequency of the converter.

A second and more critical issue is the possible loss of control of V_{cf} . As the capacitor C_f is much smaller than C , any small error in the ΔQ will lead to a significant error in ΔV . This could lead to large changes in the voltage across the capacitor with a small change in ΔQ . Again, as the number of levels of the converter is increased, controlling these voltages would become quite challenging.

6.4.1.2 CONTROL USING A SMALL-RATED TRANSFORMER

To simplify the control problem, a method has been proposed, where a small-rated transformer is used to control the voltage across the capacitor, as shown in Figure 6.10.

The transformer is used to maintain the fundamental component of the voltage at the desired value. Under no-load conditions this is quite straightforward as the voltage is impressed on the capacitor by the transformer.

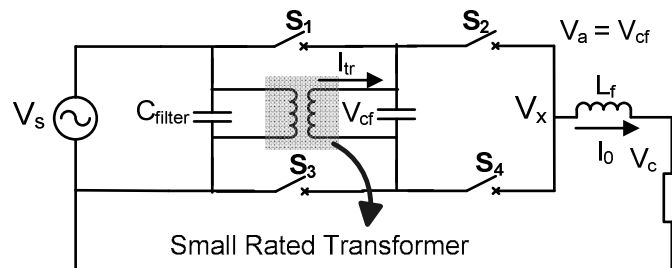


Figure 6.10: 3-level direct AC converter with small-rated transformer

However, operation during switching transients is fairly involved. Based on the mode of operation selected, the capacitor either charges or discharges

causing a ripple on the 60 Hz component of the voltage across the filter capacitor C_f . It is important to ensure that the net charge taken away or added to the capacitor is zero. This is done by the proper selection of the mode of operation. In principle, operation of the 3-level converter with the transformer is a simple solution to regulating the voltage on the C_f .

There are two concerns with this approach. The first is the relative sizing of the transformer with respect to the converter rating. This is important as it impacts both cost and reliability. Increasing the number of levels in the converter brings to light the second issue. With every additional level an additional transformer is required with a different turn's ratio and rating. This is undesirable once again due to the added cost, complexity, size, and weight of these transformers.

The following example is a simple design exercise that highlights factors influencing the rating of the transformer and the relative size of the transformer.

Consider the 3-level AC converter with operating conditions given in Table 6.4.

Table 6.4 Converter ratings for design of transformer

Converter kVA	10kVA
Switching frequency	3kHz
Input voltage	277Vrms
Filter capacitor voltage	$V_a = V_s/2 = 138\text{Vrms}$
Maximum voltage ripple	10%

The worst-case ripple seen across the filter capacitor C_f voltage is when $D = 0.5$

$$C_f = \frac{I_0 \Delta t}{\Delta V} = 260 \mu F \quad (6.5)$$

Here, C_f is the filter capacitor, I_0 is the load current, Δt is the time required per switching cycle to control V_{cf} , and ΔV is the voltage ripple across C_f .

For this value of capacitance, the transformer rating required to maintain the 60 Hz component of the voltage is:

$$VA_{Xmer} = V_a / tr = 1.88 \text{ kVA} \cong 2 \text{ kVA}$$

This is roughly 20% of the rating of the converter and will result in a transformer with a significantly large size and weight.

Simulation results to validate operation of the converter using the transformer for control of the intermediary voltage are shown in Figure 6.11. The 3-level direct AC converter (buck) has been simulated to validate the control method described. Results show the input, intermediary, and output voltage regulated to the desired values of 480, 240 and 300V respectively. The ripple on the capacitor voltage V_{cf} indicates the points of transitions between the various modes of operation that lead to charging and discharging of the capacitor.

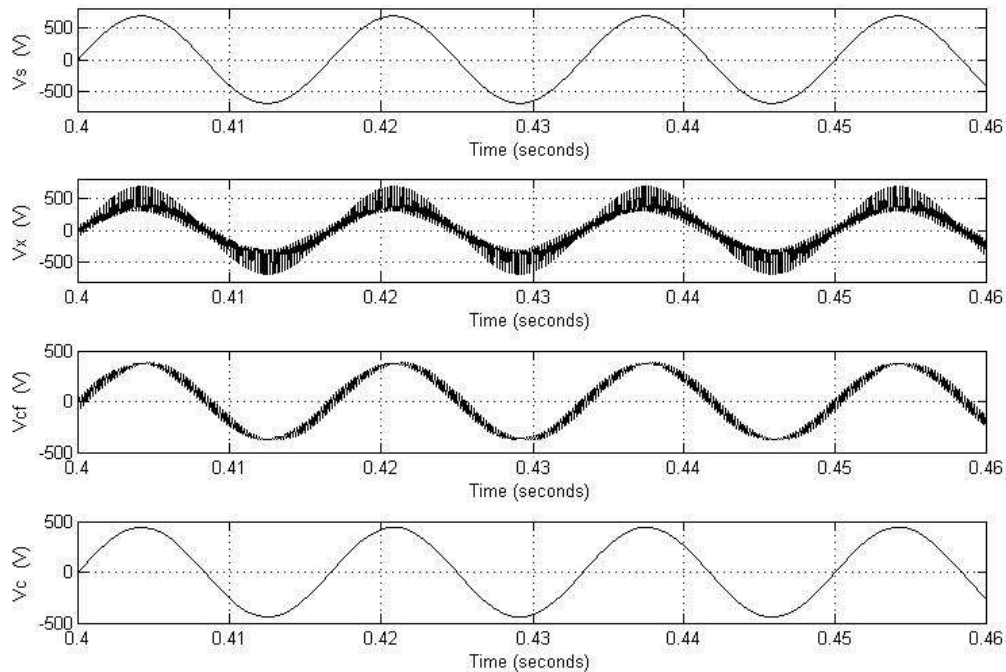


Figure 6.11: Simulation results (a) V_s , (b) V_x , (c) V_{cf} , (d) V_c

6.4.1.3 STATE-BASED CONTROL

State-based control of the converter is a novel technique that uses the modes of operation of the converter to synthesize the desired voltages in a manner similar to space vector modulation for inverters.

As an example consider once again the 3-level converter configured as a buck cell. There are essentially two capacitors across which voltages need to be controlled as shown in Figure 6.12(b).

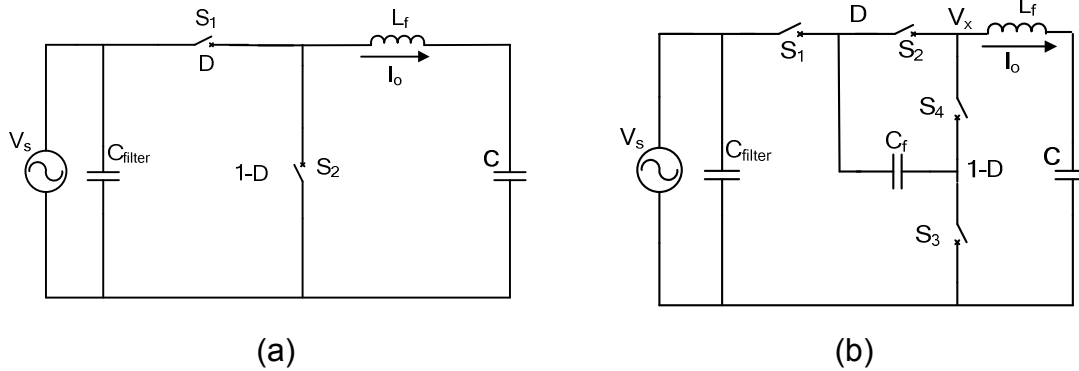


Figure 6.12: 3-level buck converter (a) 2-level, (b) 3-level

The converter has been redrawn to help visualize the similarity between a simple 2-level buck converter and a 3-level buck converter.

The first is a large capacitor, C , and the second a filter capacitor, C_f , which is a fraction of C . Once again it is important to emphasize that the filter capacitor is required for voltage balancing and is not an energy storage element. The voltage across C_f is synthesized by using the different modes of operation, described in a previous section.

1. Mode 1 generates ΔV across C
2. Mode 2 generates $\Delta V/2$ across C_f
3. Mode 3 would be a freewheeling mode

Every switching cycle needs to be divided between the three modes of operation. The following example is used to illustrate the method.

Input voltage of the converter $V_s = 480V$.

Output voltage of the converter $V_o = 300V$.

The converter operates at a switching frequency $f_{sw} = 10 \text{ kHz} = 100 \mu s$

The duty cycle of operation for the converter, D is equal to the ratio of output to the input voltage,

$$D = 0.625 = \frac{V_o}{V_s} = \frac{300}{480}$$

The first step in this control method is to determine the amount of time the converter needs to spend in mode 1, i.e., the duty cycle of the converter. Given

$D = 0.625$, the converter would need to operate in mode 1 for $62.5 \mu\text{s}$, i.e. 62.5% of each switching cycle.

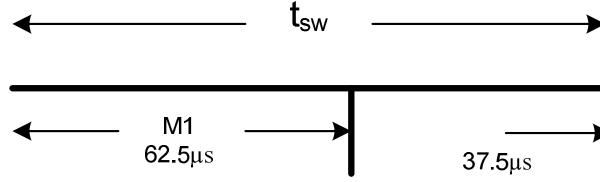


Figure 6.13: Switching cycle for state-based control

This leaves $37.5 \mu\text{s}$ that can be used to synthesize the desired voltage across C_f . Assuming the current I_o is constant over one switching cycle, the following equations can be used to determine Δt_2 , i.e., the (amount of time to be spent in mode 2).

$$I_o = C_f \frac{\Delta V_{cf}}{\Delta t_2} = C \frac{\Delta V_c}{\Delta t_1} \quad (6.5)$$

$$V_c = D \cdot V_s, \text{ and } V_{cf} = \frac{V_s}{2} \quad (6.6)$$

$$\Delta t_1 = 12.5 \cdot \Delta t_2 \quad (6.7)$$

Here, $C_f = C/10$, Δt_1 is the time spent in mode 1, Δt_2 is the time spent in mode 2, C_f is the filter capacitance, I_o is the load current, ΔV_c is the incremental increase in voltage across C , and ΔV_{cf} is the incremental increase in voltage across C_f .

Therefore to synthesize the desired voltage V_o and V_{cf} the following timing diagram is used.

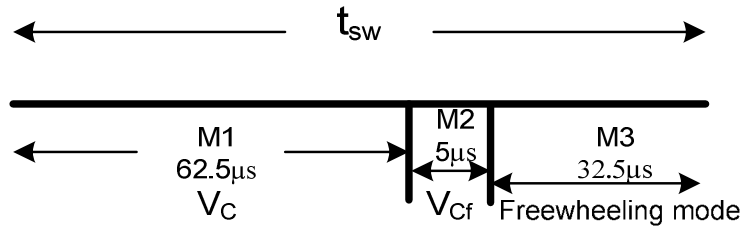


Figure 6.14: Timing diagram for 3-level converter using state-based control

The method described is similar in thought to conventional space vector modulation in VSC's, where each switching cycle is fractioned to synthesize the desired voltage. The relative sizing of the capacitors is a major factor influencing the control method.

The control method can be easily extended to more levels. An increase in levels increases complexity of the control method. The proposed control technique has been verified in simulation using a 3-level converter. The results are shown in Figure 6.15.

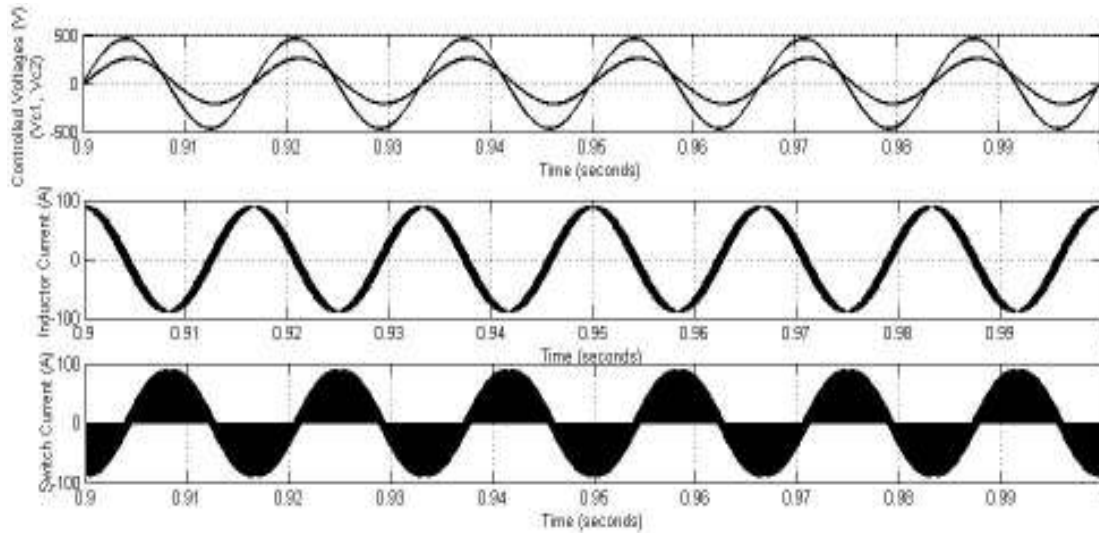


Figure 6.15: Simulation results for 3-level converter using state-based control

The converter output voltage is controlled to 300V (as in the design example). Regulation of the voltage V_{cf} to 240V with an input voltage of 480V can be seen. The proposed method is novel in that it utilizes the characteristics of the converter to its advantage, i.e., the small size of the capacitor C_f is critical in implementing this technique. Also there are no additional components necessary to implement the control method. In applications where the intermediate capacitor C_f is comparable in size to the output capacitor C , the voltage V_{cf} can be controlled to the desired value by increasing the time spent in mode 2. This results in a larger ripple on the voltage V_{cf} .

The same technique can be applied to a 3-level boost cell shown in Figure 6.16. The 3-level boost cell is used when a boost (increase) in the output voltage is desired.

Formulation of the control technique is exactly as described for the buck cell. In this case the output voltage is controlled to V_c , and the voltage across C_f is controlled to $V_c/2$. The equations for the boost cell are,

$$I_o = C_f \frac{\Delta V_{cf}}{\Delta t_2} = C \frac{\Delta V_c}{\Delta t_1} \quad (6.8)$$

$$V_c = \frac{V_s}{1-D} \text{ And } V_{cf} = \frac{V_c}{2} \quad (6.9)$$

In this example $V_c = 1.2V_s$, which corresponds to $D = 0.167$.

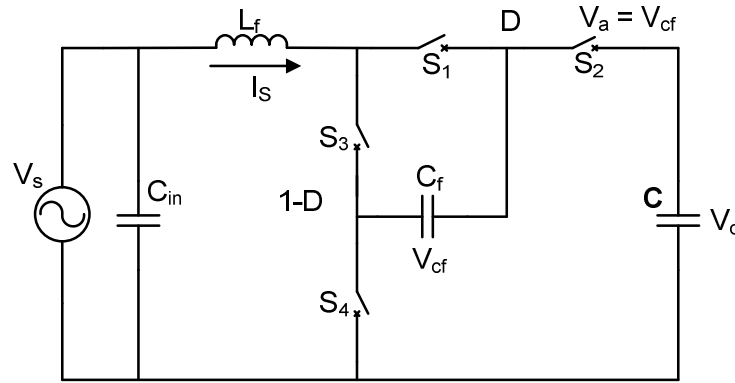


Figure 6.16: 3-level direct AC converter- boost cell

The timing diagram shown in Figure 6.17 is calculated for each switching cycle of the boost cell.

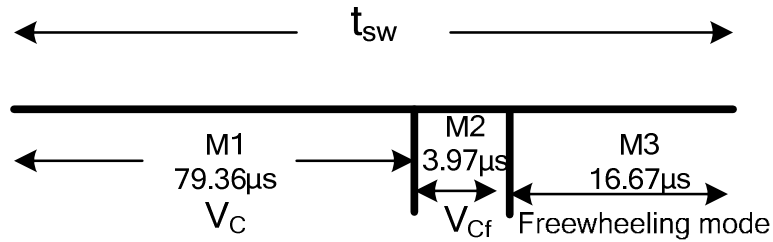


Figure 6.17: Timing diagram for 3-level converter (boost) using state-based control

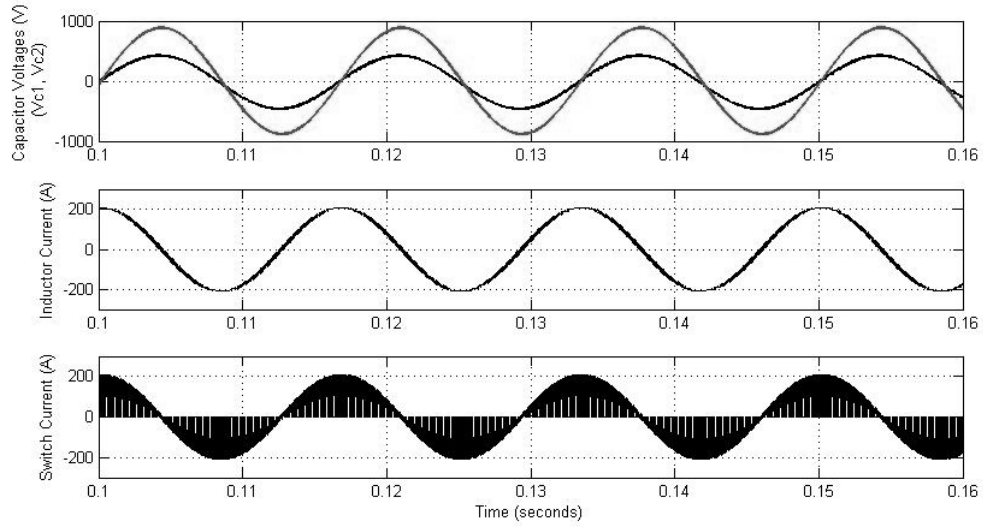


Figure 6.18: Simulation results for 3-level boost converter using state-based control

Simulation results shown in Figure 6.18 validate the timing diagram shown in Figure 6.17. The boost converter is operated to synthesize an output voltage of $V_c = 1.2V_s$. The capacitor voltage V_{Cf} is regulated to $V_c/2$.

6.4.2 IMPLEMENTATION OF THE 3-LEVEL BUCK CONVERTER

Issues with implementation of the direct AC converter are discussed in this section. The control methods discussed so far assume safe commutation between switches. Commutation in AC-AC converters is significantly more complex compared to dead time-based commutation in VSCs. Because of the complex commutation techniques, AC switches typically require snubbers.

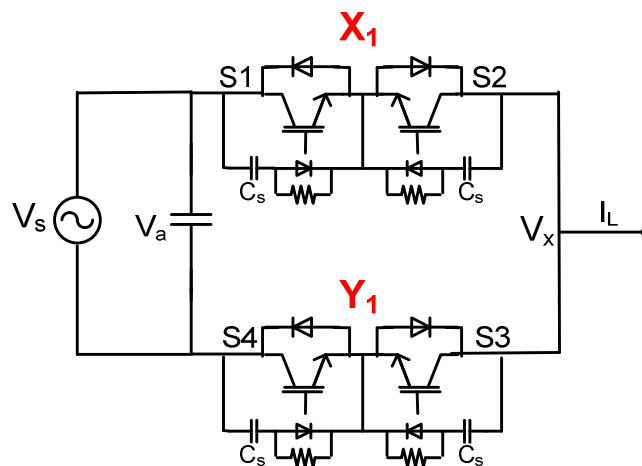


Figure 6.19: AC chopper

The use of snubbers allows for errors in commutation sequences and also protects the switches during faults. Extensive work has been done in the area of AC switch sequencing [65], [66]. Researched methods are divided based on the parameter used in determining switch sequences, such as voltage and current commutation. In the case of current commutation the direction of current determines the order in which switch transitions take place.

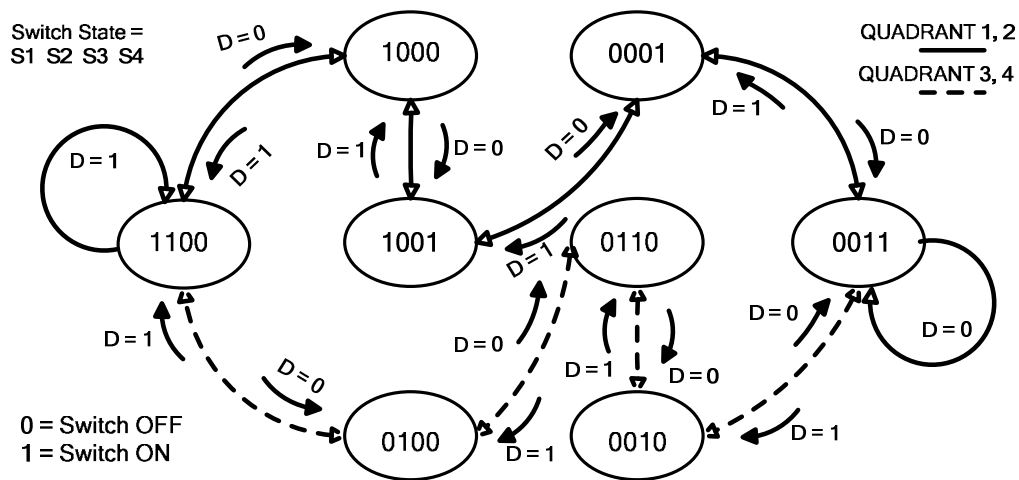


Figure 6.20: State diagram for single-phase AC chopper

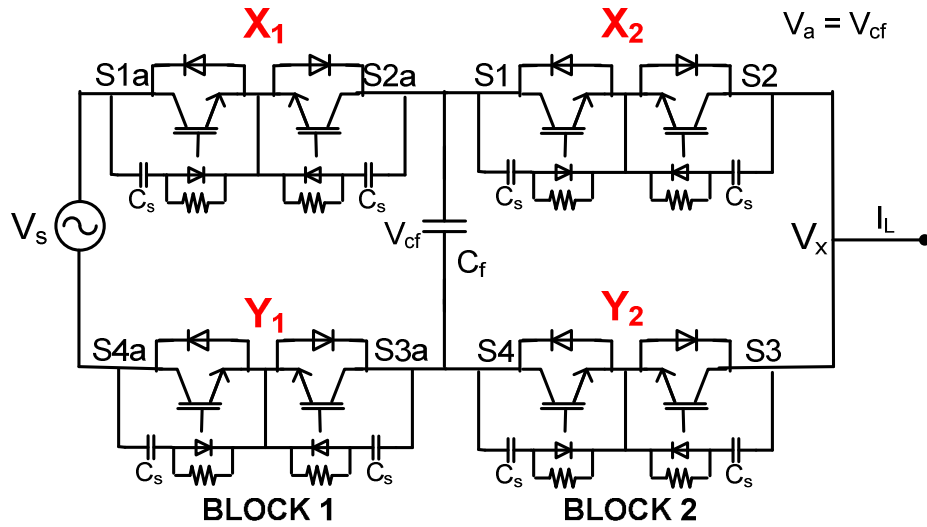


Figure 6.21: 3-level buck converter

Extending this switch commutation technique to the multilevel converter is non-trivial. The complexity as well as the possible modes or states for the converter is doubled. A complete state machine has been designed for the converter to ensure correct commutation based on current direction. Details on the structure of the state machine are included in Chapter 10.

To simplify control and sequencing, the 3-level converter is divided into two blocks; each block is an AC chopper. Transition from one state to the next for the 3-level converter is done using minimum switch transitions while maintaining the capacitor voltage and the output voltage at the desired values. The state diagram for the 3-level converter is shown in Figure 6.22(a), where each AC switch is treated like a single device.

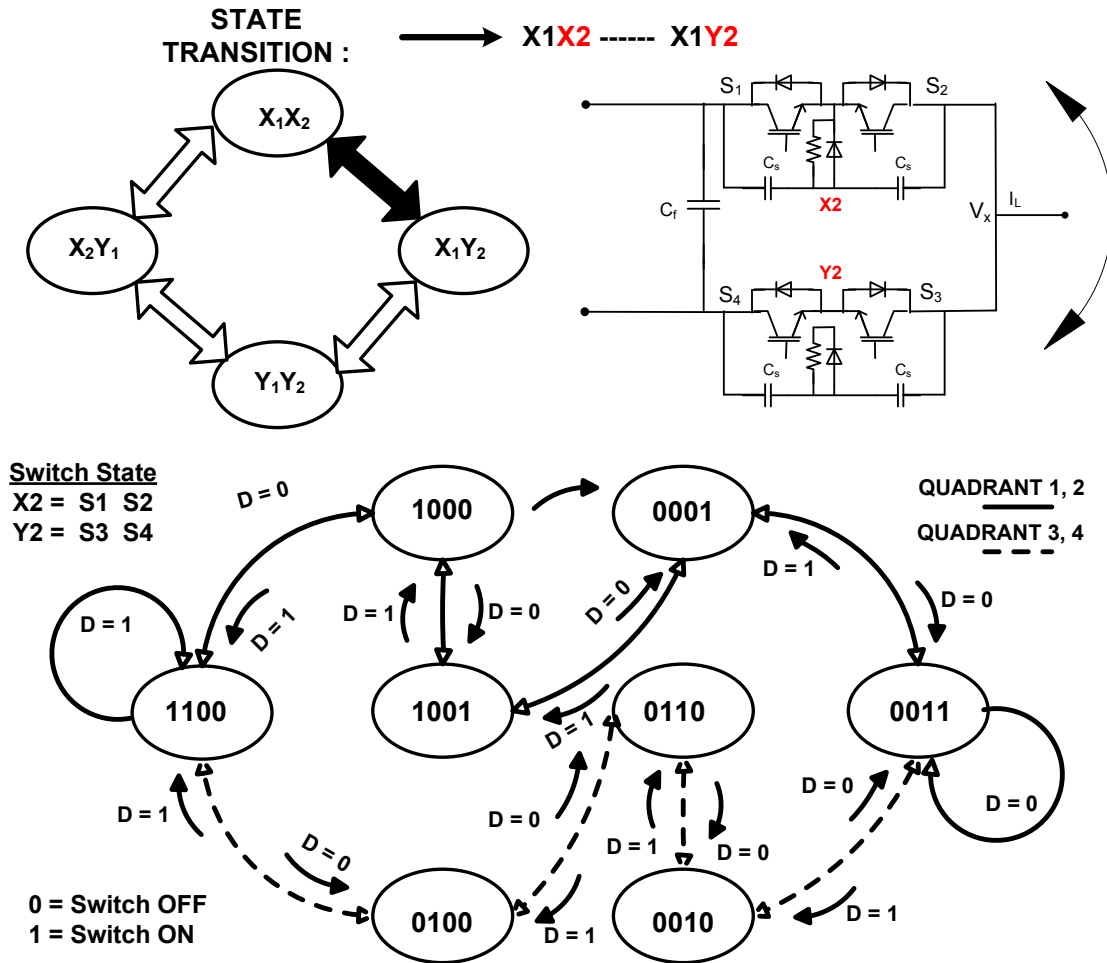


Figure 6.22: 3-level buck converter (a) AC switch state diagram with state transitions on a device level

During any one switching period, only one block is switched, while the other remains in its present state. Each state transition in Figure 6.21 is a four-step commutation sequence, as shown for the AC chopper in Figure 6.20.

To provide clarity, one state transition for the 3-level converter is illustrated in Figure 6.22, i.e., transition from $X1X2$ to $X1Y2$. In this case block 2 makes a state transition while block 1 remains in its current state. Further details on commutation techniques will be discussed in Chapter 10.

The 3-level buck converter has been validated experimentally in the laboratory. Results showing the operation of the converter are shown in Figure 6.23(b) and 6.24. Both control techniques discussed in Section 6.4.1 have been

validated experimentally. The first set of results shown in Figure 6.23(b) illustrates the operation of the converter as a buck cell. The intermediary voltage V_{cf} is controlled using a small-rated transformer. The converter has been controlled to synthesize an output voltage (V_x) that lies between V_{cf} and V_s . The voltage V_x is the unfiltered voltage at the output of the converter. Figure 6.24 illustrates operation of the 3-level converter using state-based control, i.e., minus the transformer for voltage regulation. The voltage V_{cf} has been controlled to be equal to $V_s/2$ and $V_c = 0.625 \cdot V_s$.

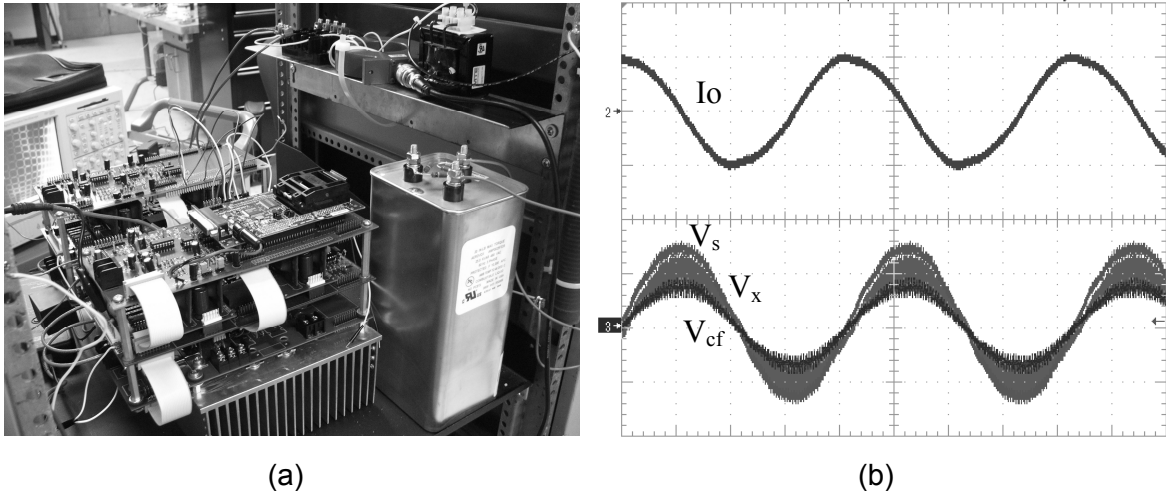


Figure 6.23: Experimental results for a 3-level buck converter (a) experimental setup, (b) control using small-rated transformer V_s , V_x and V_{cf} , (c) state-based control: output current.

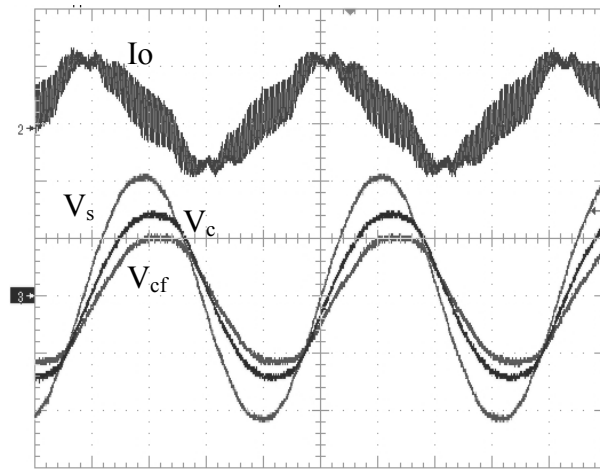


Figure 6.24: 3-level buck converter: (a) output current, (b) V_s , V_c and V_{cf}

6.5 CONCLUSION

The direct AC converter discussed is a critical part of the concept of TACC's. This chapter addresses scaling and implementation of the direct AC converter to enable direct AC conversion with no bulk energy storage elements.

The converter is realized using a cascaded structure with the AC chopper as a building block. Details of the modes of operation of the 3-level and 4-level direct AC converter have been presented. Challenges with realistic scaling and implementation of the converter have been discussed in detail. Control issues associated with scaling using multiple levels has been presented with three possible control methods. The control methods have been proposed with details on the formulation of the method as well as the pros and cons of the each solution, explained through design examples where relevant. The most promising control method is state-based control. This method has been applied to both buck and boost direct AC converters. It is novel in its simplicity and ease of implementation for this application. Simulation and experimental results have been presented to validate two of the three control methods.

The multilevel direct AC converter presented in this chapter has been shown to be scalable and robust, two characteristics that are vital in the realization of TACC's.

CHAPTER 7

INVERTER-LESS STATCOMs

7.1 INTRODUCTION

The concept of an Inverter-less STATCOM (ILSTATCOM) will be presented in this chapter. The ILSTATCOM is an application of TACC's. The concept has been presented briefly in Chapter 4. The ILSTATCOM is realized using gate turn-off semiconductor switches, which are configured in direct AC-AC structures along with VAR compensation capacitors to realize the desired functionality. The goal here is to develop a device that provides the functionality of a STATCOM without the DC-AC converter and energy storage.

The objective of the ILSTATCOM is to use existing VAR compensation capacitors to provide dynamic, controllable VARs. Under nominal voltage the ILSTATCOM is designed to deliver fully controllable capacitive VARs from zero to a maximum design value. By adding a suitably rated inductor, the VARs can be shown to vary over a lagging to leading value as desired. Under low line voltage conditions, typically occurring during system faults, the effective capacitance connected to the grid can be increased to be able to maintain a maximum value of leading reactive current with which to support the grid.

The principle of operation, design and scaling methods of the ILSTATCOM will be discussed in detail with simulation and experimental results to validate the same.

7.2 PRINCIPLE OF OPERATION: C-BUCK AND C-BOOST CELLS

The basic principle of operation for the ILSTATCOM is described below. An AC chopper is inserted between the AC line and the shunt VAR capacitor C . The converter is generally controlled with a constant duty cycle D at a relatively high switching frequency f , as is shown in Figure 7.1(a). Higher switching frequency

components are assumed to be filtered by L_f and C_f . As D is varied, it is seen that the input of the AC chopper looks like a capacitor of value $(D \cdot C)$, which can be smoothly and rapidly varied between zero and C . Figure 7.1(c) shows the effective current drawn from the AC line as D is changed from 1 to 0.5.

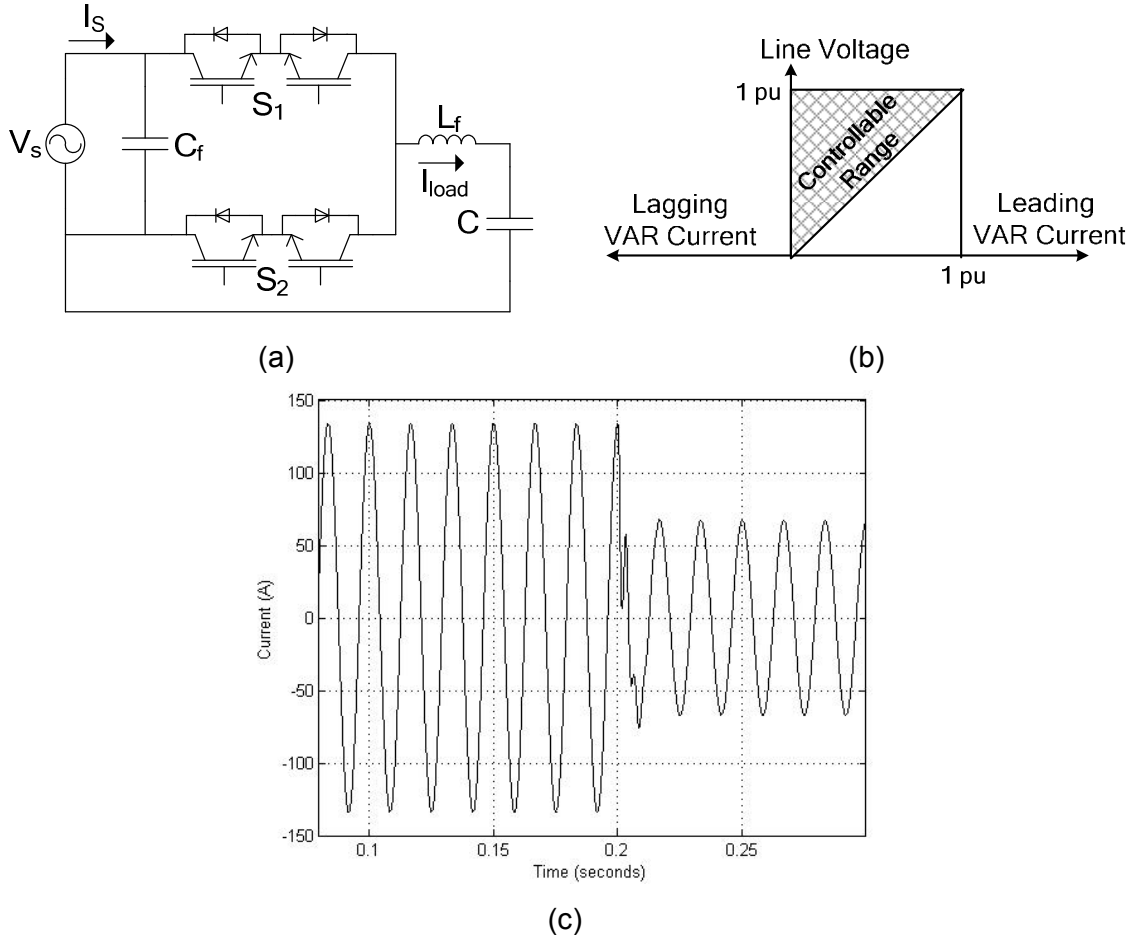


Figure 7.1: (a) Inverter-less STATCOM- buck cell, (b) effective current drawn by the buck cell for D varied between 0 and 0.5, (c) control range for buck cell

Figure 7.1(b) shows the level of control that can be obtained with the buck cell. At nominal line voltage the reactive current drawn can be varied from zero to a maximum defined value. By way of example, for a 10 MVAR ILSTATCOM realized with the buck cell, this would require 10 MVAR of capacitance. However, at a reduced line voltage, say down to 50%, this would only provide 2.5 MVAR at 50% of the leading current drawn at full voltage. This behavior is

similar to an SVC where the effective inductance is varied through thyristor phase angle control. This is clearly a limitation of applying only the buck cell.

Figure 7.2(a) shows the buck cell configured to operate backwards, i.e., as a boost cell. This cell is also controlled by varying the duty cycle D . At $D=0$, the effective capacitance obtained at the input terminals is clearly C . At finite non-zero values of D , the effective capacitance is seen to be increased to a value of $C/(1-D)$.

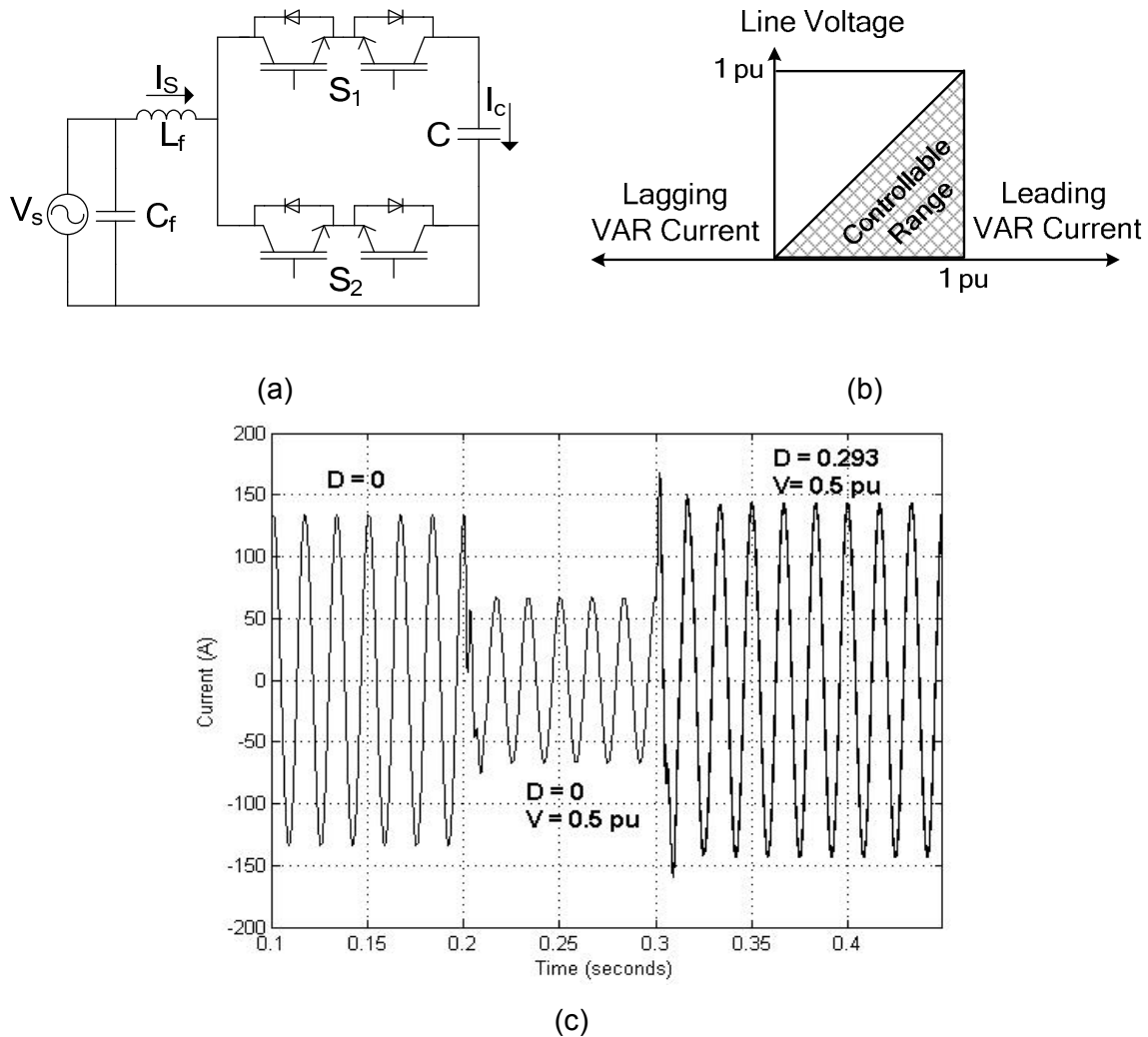


Figure 7.2(a) Inverter-less STATCOM- boost cell, (b) current drawn at an input voltage of 0.5 pu, (c) control range for boost cell

For instance, for a duty cycle of $D=0.5$, the effective capacitance would be $2C$. If the boost cell were operated with an input voltage of 50% and a duty cycle

of $D=0.5$, the effective VARs drawn by the boost cell would correspond to the VARs drawn by C at full line voltage. This would also correspond to 2 pu current being drawn from the line, resulting in higher current stress for the semiconductor switches. Alternatively, setting the duty cycle to 0.293 limits the reactive VAR current drawn to 1 pu, mimicking the behavior of a STATCOM.

Figure 7.2(c) shows the line current drawn by the boost cell in response to voltage sag to 0.5 pu, and Figure 7.2(b) illustrates the range of control for the boost cell.

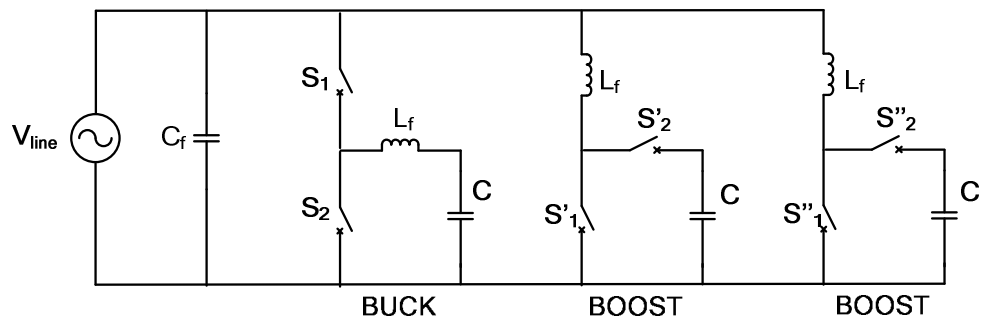
7.3 INVERTER-LESS STATCOM IMPLEMENTATION

The ILSTATCOM functionality can thus be realized using a combination of buck and boost cells. For instance, Figure 7.3 shows one buck and two boost cells used to realize an ILSTATCOM. Each is assumed to be rated at 3.33 MVAR at nominal voltage. At nominal line voltage, the buck cell is used to provide control from 0 to 3.33 MVAR. When a higher level of VARs is required, the boost cells are switched in as needed. This adds a fixed 3.33 or 6.66 MVARs to the overall compensation, allowing the buck cell to control the final value to a maximum of 10 MVARs as needed. Further, as the capacitors and switches need to be sized for continuous duty up to 120% line voltage (potentially encountered under normal line connected operation), the boost cells could provide additional VARs under nominal line voltage by boosting the capacitor voltage to 1.2 pu. In this case each boost cell could provide 4.8 MVARs for a total of 12.9 MVARs at nominal line voltage, or 30% more than possible with the fixed capacitors. This increase in the nominal VAR rating has a big impact on the cos per MVAR of the ILSTATCOM.

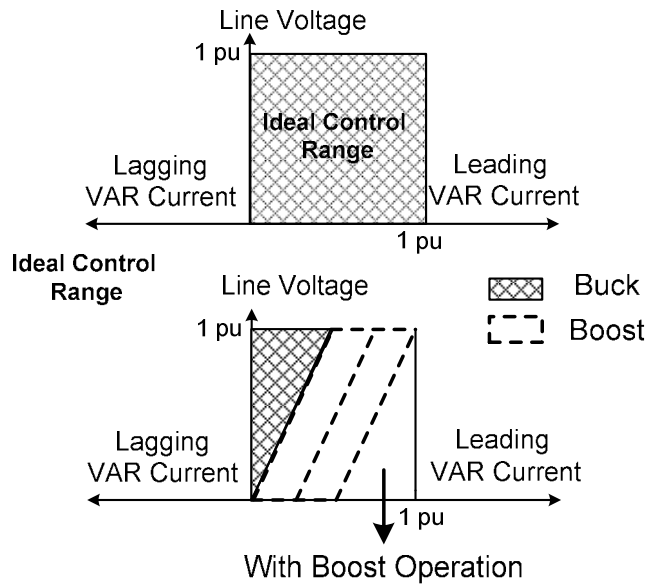
Under low line voltage conditions, the boost cell can be operated in the boost mode to realize a higher effective capacitance value, and higher VARs. For instance at 50% input voltage, the combination of the buck and boost cell can realize a total of 5 MVARs with boost to 1 pu capacitor voltage, or 6 MVARs with boost to 1.2 pu voltage. Figure 7.3(b) shows the control range achievable by the ILSTATCOM configured as shown in Figure 7.3(a). It demonstrates that the

ILSTATCOM can provide 0 to 1 pu leading current over a wide range of line voltage, very similar to a STATCOM.

It should be noted that the use of gate turn-off switches for the switches (S_1 , S_2 etc) allows insertion of the desired capacitance value at any arbitrary point-on-wave of the line voltage. For instance, on receiving an 'insert capacitance' command, the switches can operate in a current regulated mode at maximum permissible current until the capacitor voltage attains the desired value. Unlike an SVC, this allows very fast (sub-cycle) response time. Also, unlike an SVC, the ILSTATCOM elements can be rapidly turned off.



(a)

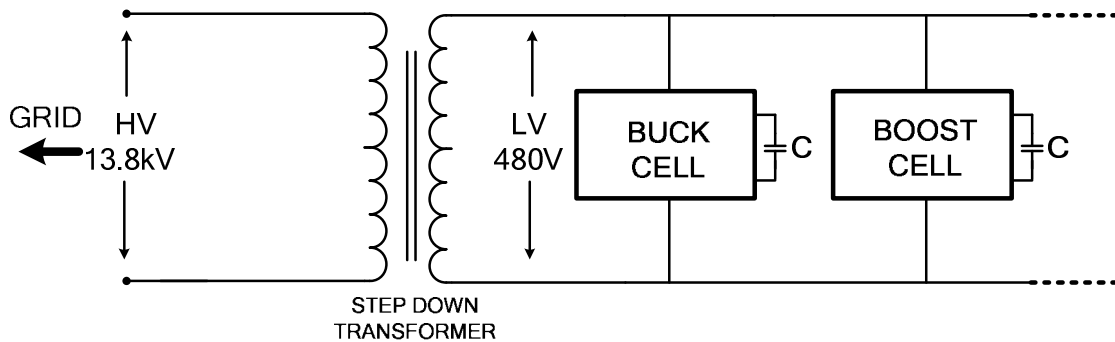


(b)

Figure 7.3(a) Inverter-less STATCOM, (b) ideal control range and achievable control range

7.4 SYSTEM CONSIDERATIONS

Implementing a full scale ILSTATCOM from buck and boost cells can be done using one of several different approaches. The ILSTATCOM can be implemented using a certain number of paralleled low voltage AC chopper modules configured in buck or boost mode as required, with the whole group connected to the high voltage line through a transformer. This is similar to the DVAR product from American Superconductor, and represents a common technique that is simple to implement, and does not require high voltage power electronics [6]. However, transformer costs can be significant, especially when interfacing to the high voltage grid. It also limits the size and rating of individual single-phase modules to around 400 kVAR, and of the overall system to ~10-15 MVAR. Finally, issues of transformer saturation under certain types of asymmetrical faults can limit the efficacy of transformer based STATCOMs [12]. Figure 7.4 shows an example of a transformer-coupled ILSTATCOM. The simulation results show operation of ILSTATCOM with one buck and one boost cell. Each cell is rated at 400kVAR. The total VARs generated by the ILSTATCOM is 1.28MVAR.



(a)

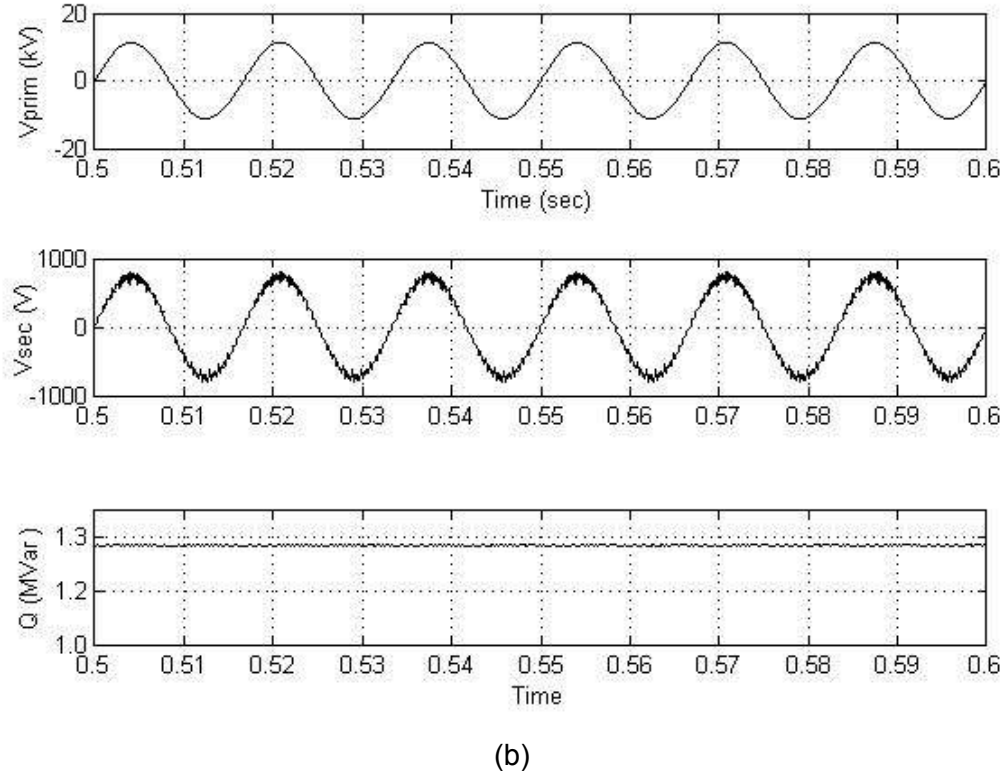


Figure 7.4: Transformer-coupled ILSTATCOM: (a) schematic, (b) simulation results

Higher voltages can be achieved by series stacking of cells. This method would eliminate the transformer and lower the cost and losses of the ILSTATCOM. Two distinct approaches are possible. The first involves a simple stacking of individual buck and, or boost cells, with a small-rated transformer providing a voltage balancing circuit. If we assume operation of say five stacked C-buck cells operating as shown in Fig 7.5, the cells can be controlled so as to dynamically share voltage.

However, when the duty cycle D is zero, with the ILSTATCOM providing minimum VARs to the line, it is critical that the voltages across the semiconductors be balanced. This function is provided by the filter capacitors C_f in each module. Figure 7.5 shows the basic design of a stacked buck cell, including how the transformer can be integrated into the basic module. A similar stacking arrangement and operating principle is proposed for the stacked boost cells. Taken together, it is possible to realize a transformer-less ILSTATCOM suitable for medium voltage applications.

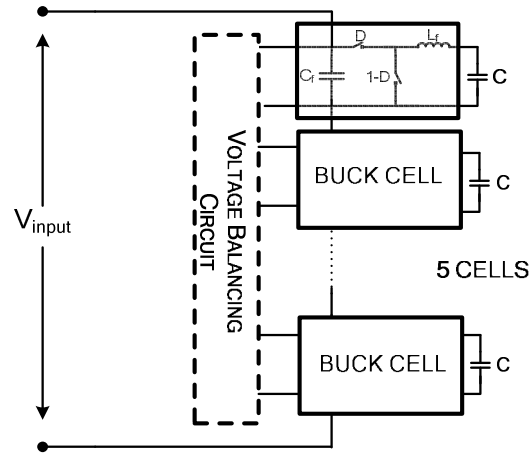


Figure 7.5: Schematic of single-phase implementation of STATCOM with buck cell

Figure 7.6 extends the idea of series stacking cells to a full STATCOM with two series stacked boost cells and one series stacked buck cell. Each cell operates with a PWM control strategy that can incorporate VQS modulation for harmonic control [7, 8]. Consider 1700 V, 1000 A IGBTs, this can implement a 4.8 MVAR IL-STATCOM system at 4.16 KV with a four-stage stack of IGBTs incorporating one buck cell and two boost cells per-phase. A detailed design example will be presented in a later section.

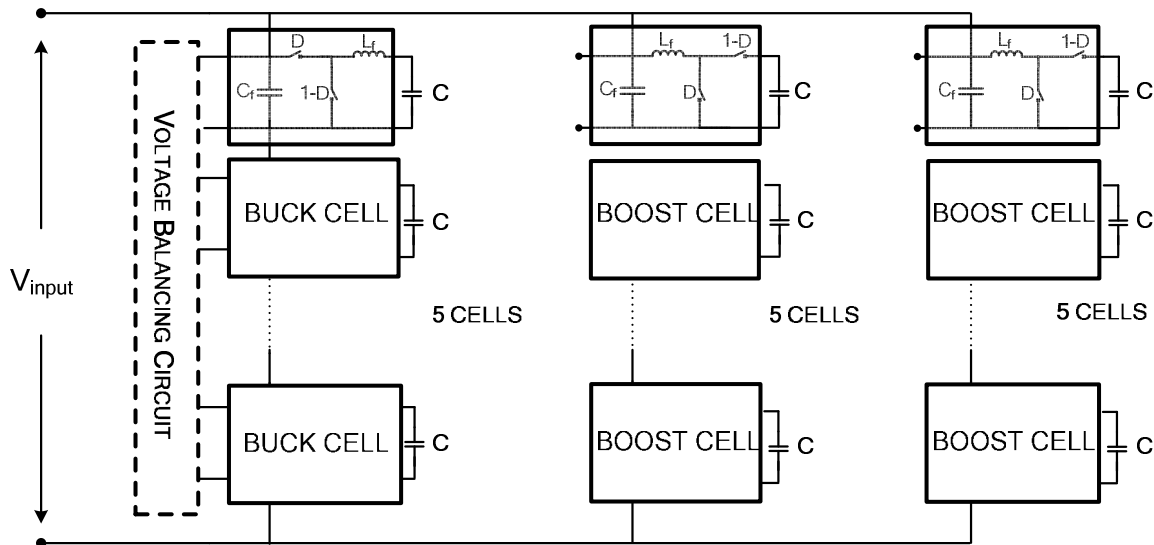
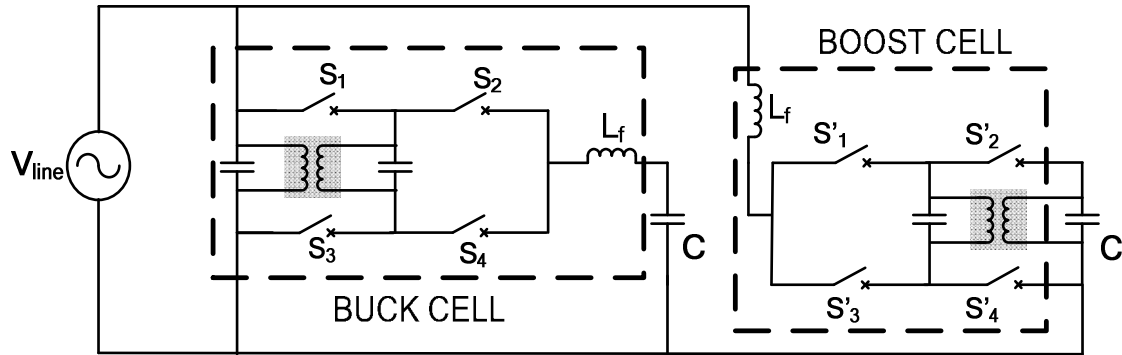
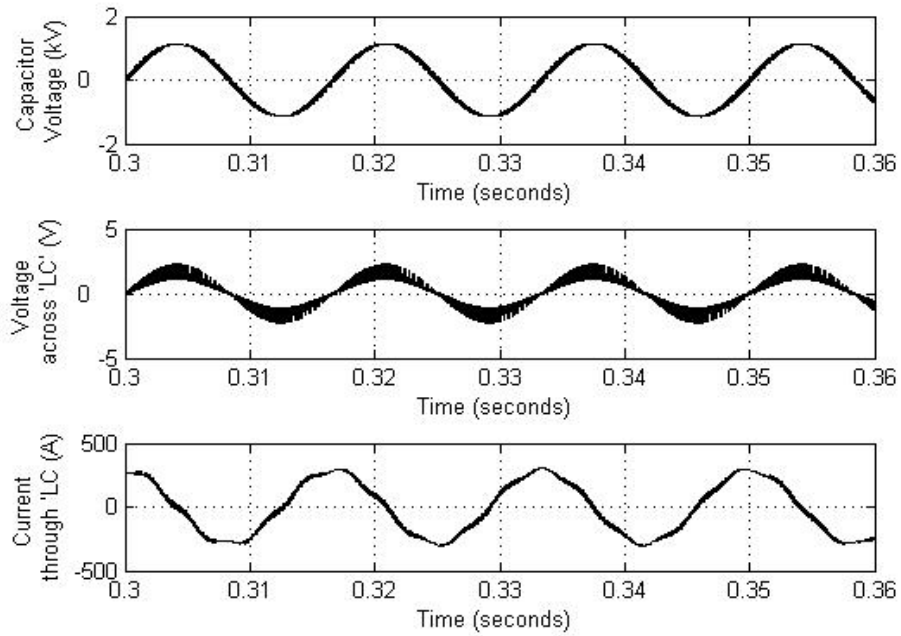


Figure 7.6: Schematic of single-phase implementation of series stacked ILSTATCOM with one C-buck Ccell and two series stacking arrangements of C-boost cells

The third and final approach to scaling the ILSTATCOM is using the concept of TACC's [11]. Augmenting an existing VAR compensation capacitor with a multilevel direct AC converter (discussed in Chapter 6) would allow for scaling of the ILSTATCOM. Figure 7.7(a) shows an example of a 3-level direct AC converter that is used to realize an ILSTATCOM, while Figure 7.7(b) shows typical switching waveforms obtained using simulation. The TACC can be implemented with a higher number of switching levels to realize higher system voltages.



(a)



(b)

Figure 7.7: (a) 3-level direct AC converter topology (ILSTATCOM), (b) switching waveforms for 3-level buck cell

For instance, a four level TACC using 1700 V 1000 A IGBTs could realize a three-phase 4.8 MVAR transformer-less ILSTATCOM at the 4.16 kV level using available VAR compensation capacitors.

The concept of the buck and boost cell has been experimentally verified with a laboratory scale prototype, as shown in Figure 7.8(a). Figure 7.8(b) shows waveforms illustrating operation of the 3-level ILSTATCOM using 1200V, 100A IGBTs. Further development has been carried out in the design and fabrication of a MV ILSTATCOM prototype described in Chapter 10.

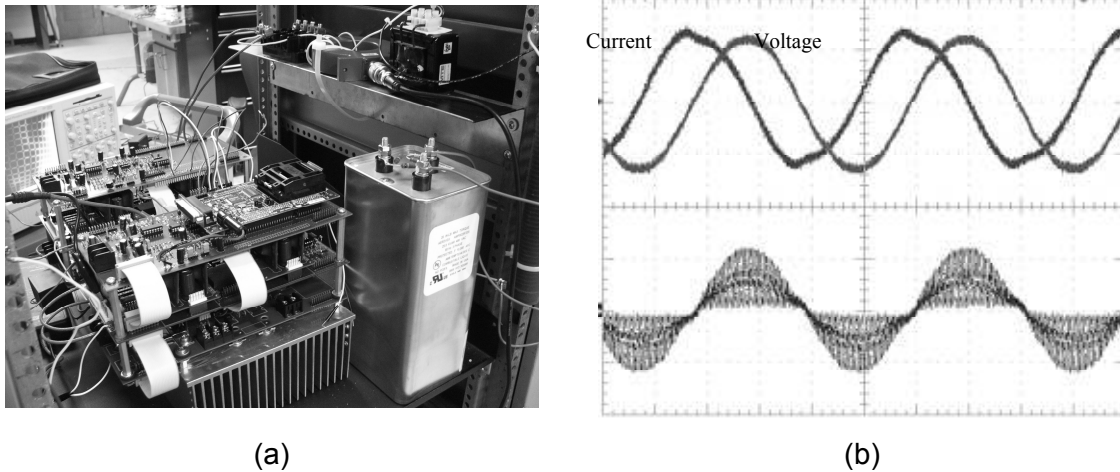


Figure 7.8: (a) Experimental setup for 3-level direct AC converter topology - ILSTATCOM, (b) input voltage (V) and output current (A), output voltage (V).

Figure 7.8(b) shows the input voltage and output capacitor current. These two parameters have been used in determining the quadrant information for operation of the converter. Details of implementation, including the switching sequence for the IGBTs, have been discussed in Chapter 6. Figure 7.8(b) clearly illustrates the operation of the multilevel AC converter in an ILSTATCOM implementation. The different levels in voltages that are used in synthesizing the desired output voltage can be seen. Figure 7.8(b). The converter has been controlled to transition through all the possible states in order to illustrate the operation of a 3-level AC-AC converter.

7.5 DESIGN CONSIDERATIONS

The design of the proposed ILSTATCOM is discussed and compared with existing SVC and STATCOM solutions, for a baseline design of 0.5MVAR lagging to 4.8 MVAR leading of dynamic compensation at 4.16 kV.

The SVC would require a 5.3 MVAR reactor to achieve the desired rating, while the ILSTATCOM would need 0.5 MVAR. The conventional STATCOM can intrinsically provide lagging or leading VARs, and does not require a reactor.

It should be noted that a basic inverter cell used as the building block for a STATCOM has a total ideal device rating of $(4.V_p.I_p)$, where V_p is the peak voltage of the DC bus, and I_p is the peak capacitive current. For the ILSTATCOM, in both buck and boost configurations, the total ideal device rating is the same at $(4.V_p.I_p)$. Further, the VAR rating for these cells is $(V_p.I_p/2)$. This is unexpected as one normally thinks of direct AC converters having a higher switch count and VA rating than equivalently rated DC-AC inverters.

The second fundamental difference is in the amount of capacitance required. Given the long life and high voltage requirements, most STATCOMs use film capacitors instead of electrolytic capacitors. A common assumption in the design of STATCOMs is that of a balanced three-phase supply, a result of inverter designs that have been derived from the world of AC drives and from an imperfect understanding of grid dynamics. This assumption results in an extremely low value of DC bus capacitance required, suggesting that the STATCOM is a lower-cost solution than is true. The vast majority of faults on the grid are asymmetrical, imposing single-phase loading on the inverter, requiring substantially larger capacitors than under a balanced three-phase scenario. By way of example, Areva's chain link STATCOM design accepts the unbalanced operating requirement, and provides a robust, rugged and realistic design [4].

For the ILSTATCOM, each buck or boost cell requires a total amount of capacitance that equals the VARs to be provided. For instance, for a buck or boost cell designed to provide 400 kVAR per cell at 600 V_{rms} and 700 A_{rms} , the capacitance required is 3100 μF . For the conventional STATCOM, designed for single-phase loading with similar devices and with 6% ripple on the DC bus, the

DC bus capacitance required is 52000 μ F. This is a dramatic difference, particularly given that these are the same type of capacitor.

Finally, the ILSTATCOM can provide additional VARs under nominal line conditions, as result of the boost cells. For instance, if the capacitors and switches are selected to handle a 20% line overvoltage, the ILSTATCOM can deliver 44% more VARs at 1 pu line voltage, when compared with an SVC. Other STATCOMs may also be able to offer similar overload attributes, given adequate over-rating of devices.

7.6 CONCLUSION

This chapter has presented a novel approach to implementing Inverter-less STATCOMs, or ILSTATCOMs, using shunt VAR compensation capacitors coupled with readily available IGBTs. The use of VQS PWM techniques (discussed in Chapter 5) allows dynamic VAR control and harmonic isolation functions [7]. The proposed approach can be easily scaled using a variety of approaches to implement ILSTATCOMs suitable for high power and high voltage operation.

Three distinct approaches have been presented for scaling this concept to high power levels. Two of the three concepts involve stacking of cells to realize higher voltage. The first approach uses stacked single-phase cells that show good controllability and a modular approach to implementation. The use of a low rating transformer embedded into individual modules provides a good voltage balancing function under low VAR conditions.

An alternative approach using TACC's based on multilevel AC converters has the added benefit that it can be used in retrofit applications to convert existing shunt VAR capacitors into dynamic VAR sources. Implementation issues for ILSTATCOMs based on both techniques have been discussed, and comparison with SVC and existing STATCOMs has been presented.

CHAPTER 8

SYSTEM IMPLEMENTATION

8.1 INTRODUCTION

System impact of the ILSTATCOM is studied in this chapter. The ILSTATCOM is studied using two IEEE benchmark systems. The effects of the ILSTATCOM verses conventional methods of VAR compensation have been compared using simulation results.

8.2 IEEE 13 NODE TEST FEEDER

The first system considered as part of the analysis is the IEEE 13 Node Test Feeder, shown in Figure 8.1. The system is a 4.16 kV three-phase feeder. Details on the feeder are included in Appendix A.

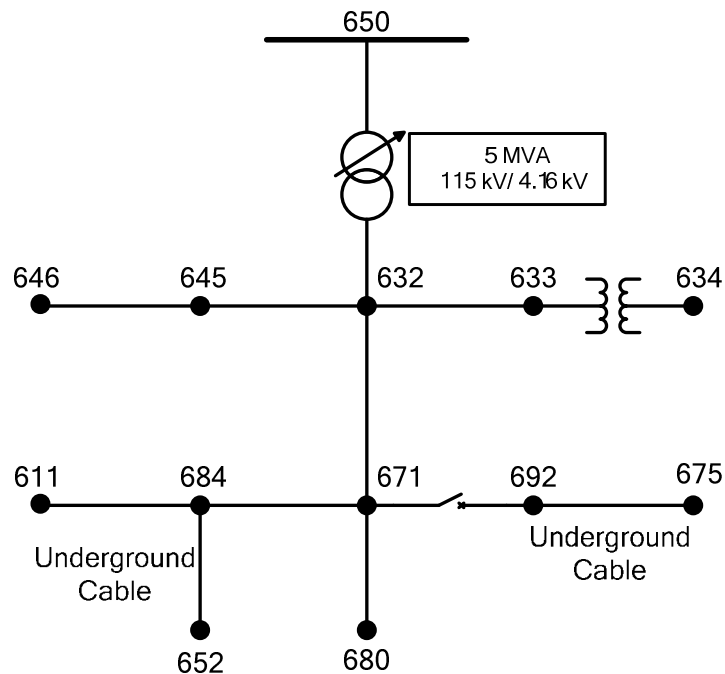


Figure 8.1: IEEE 13 node test feeder

The main components of the feeder include twelve line segments, two transformers, one voltage regulator, and two shunt capacitor banks. Multiple test

scenarios have been studied to understand the system under different operating conditions. The primary control objective for the given system is to control node voltages between 0.95 and 1.05 pu.

Figure 8.2 shows the voltage profile of the system with no compensation, i.e., no voltage and VAR regulation.

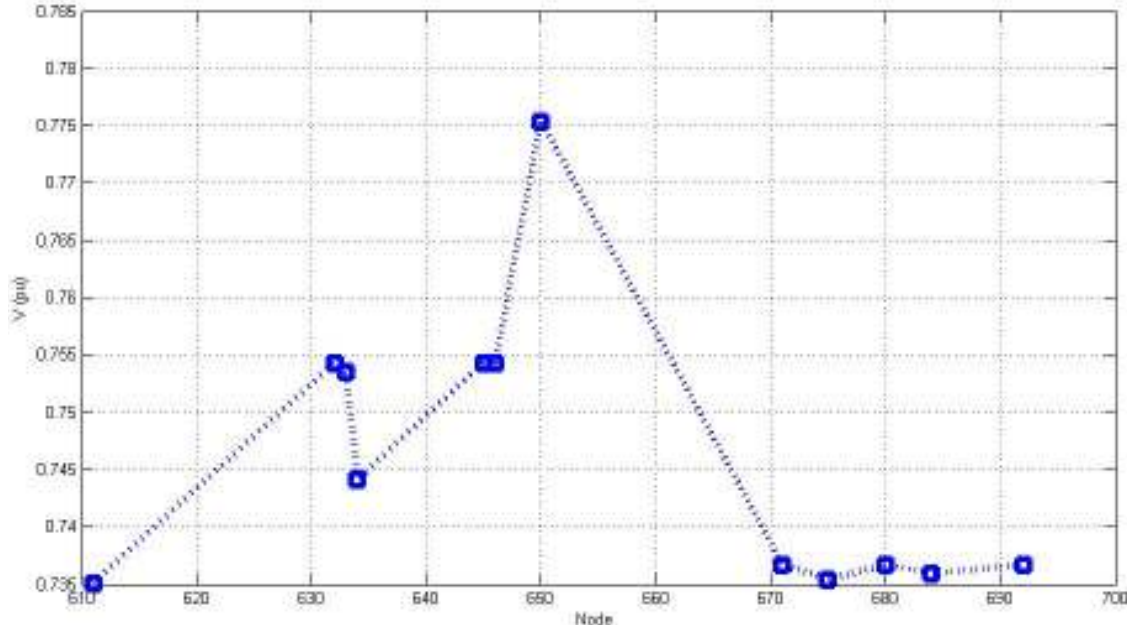


Figure 8.2: Voltage profile of uncompensated system

The voltage profile of the system can be improved by either a direct method involving voltage regulators and on-load tap changers or an indirect method that uses shunt reactive power compensation to achieve improved voltage and power factor profiles for the overall system.

The ILSTATCOM is an indirect method of voltage regulation, where the injected leading current has a direct impact on the power factor at the point of connection and an indirect impact on the voltage at the point of connection. The benchmark system includes two MSCs at nodes 611 and 675. At nominal voltage the MSCs generate 100 kVAR and 200 kVAR respectively. The improved voltage profile is shown in Figure 8.3. The analysis and simulation results shown in the following sections illustrate the advantages of using an ILSTATCOM over conventional MSC's.

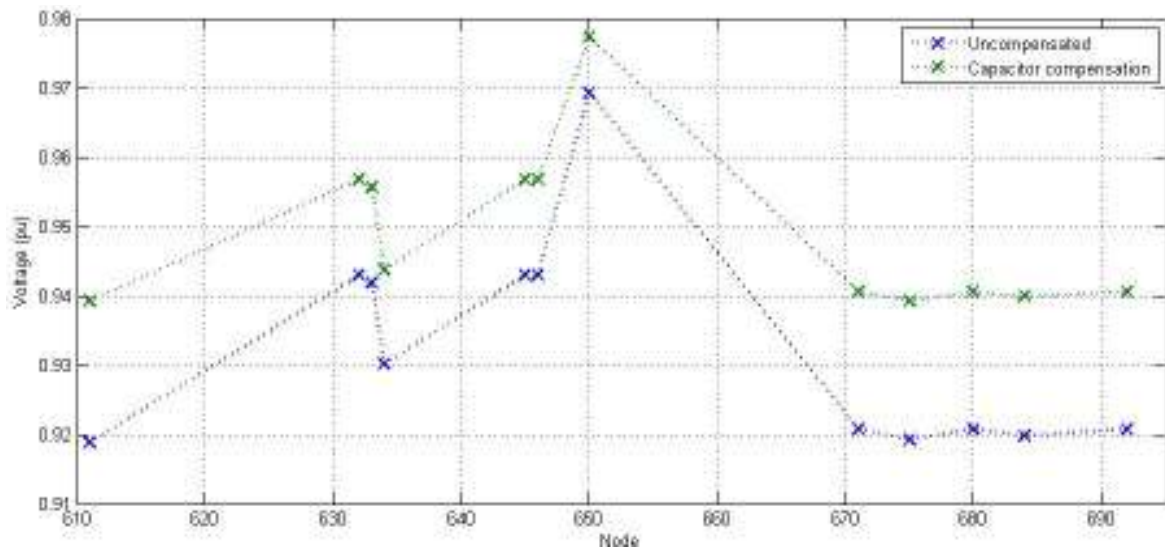
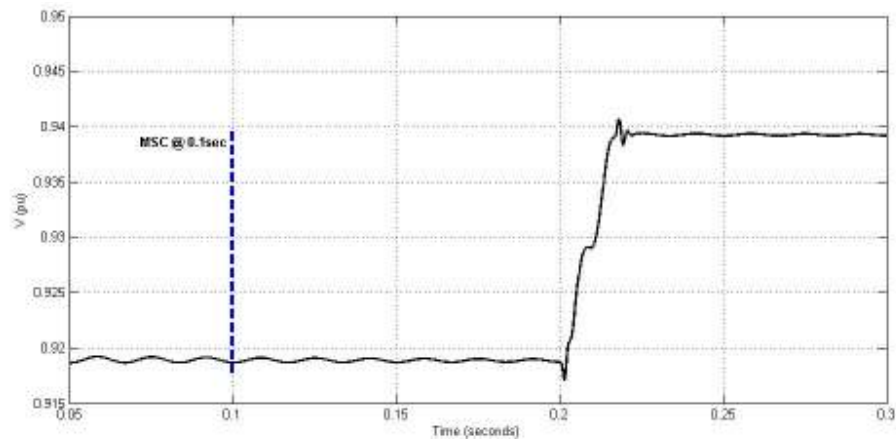


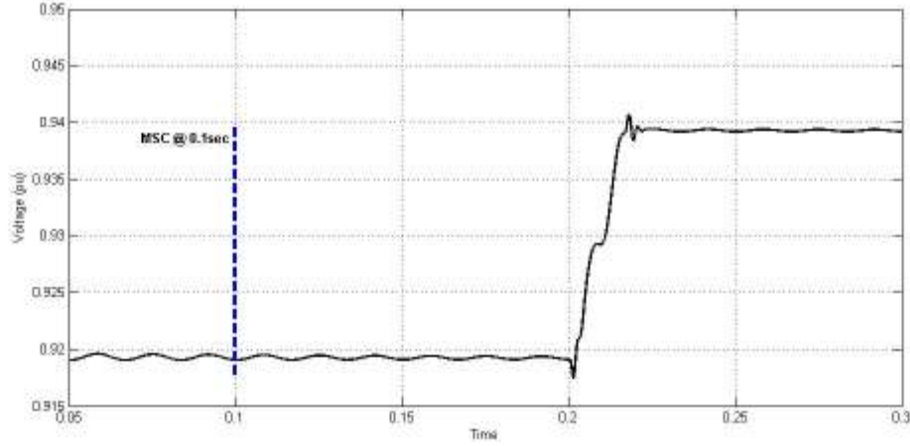
Figure 8.3: Voltage profile of system compensated with MSCs

Important characteristics of the MSC include:

1. Response time – the MSC has been modeled using data obtained from commercially available devices with switching times of up to six cycles of the fundamental ~ 100 ms.
2. Limitation of VARs – the total leading reactive power generated by the capacitors is given by V^2/X_C . The limitation is because of the fixed value of capacitance of the device.



(a)



(b)

Figure 8.4: Voltage (rms) profile with MSCs: (a) node 611, (b) node 675.

The buck and boost cells have the same value of capacitance used in the MSC. In theory the buck cell is effectively an MSC with a better response time. Considering high frequency filter components in the converter, the overall VARs generated by the buck cell increase. The following equations and analysis quantify the improvement in VARs.

For a filter capacitor with capacitance equal to C_f ,

$$\text{Reactive power generated by buck cell} = \frac{V_s^2}{X_{cf}} + \frac{V_c^2}{X_c} \quad (8.1)$$

$$\text{Voltage across capacitor } C = V_c = D \cdot V_s \quad (8.2)$$

Where, V_s is the input voltage, V_c is the voltage across the MSC, X_{cf} is the reactance of the filter capacitor at 60Hz, and X_c is the reactance of the MSC.

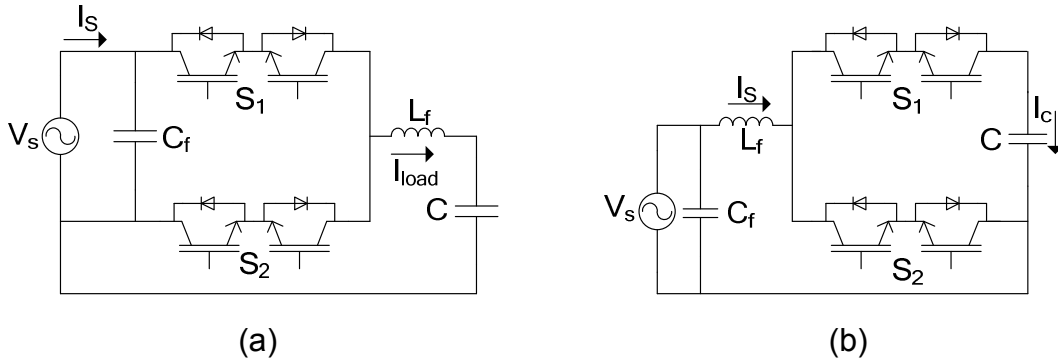


Figure 8.6: Schematics for buck and boost cell: (a) buck, (b) boost

The value of filter capacitance has been selected to maintain the ripple on the input voltage to be below 10%.

Similar analysis is valid for the boost cell, with the voltage across the capacitor C.

$$V_c(\text{boost}) = \frac{V_s}{1-D} \quad (8.3)$$

Where, V_c is the voltage across the MSC and V_s is the input voltage.

For the given the ratings of the capacitors in the test system with the additional filter capacitors, VARs generated by the different reactive power compensation devices are calculated and shown in Table 8.1.

Table 8.1: Compensation at nodes 611 and 675 using MSCs, buck, and boost cells

Theoretical Values			
Compensation at 1.0pu	MSC	Buck (D = 1.0)	Boost (D = 0.2) V _c = 1.25 pu
Node 611	100 kVAr C = 15.36μF	230.7 kVAr C _{buck} = 15.36μF C _f = 20 μF	287.1 kVAr C _{boost} = 15.36μF C _f = 20 μF
Node 675	200 kVAr C = 30.72μF	330.9 kVAr C _{buck} = 30.72μF C _f = 20 μF	443.64 kVAr C _{boost} = 30.72μF C _f = 20 μF
Simulation Results			
Compensation at V (pu)			
Node 611	V = 0.9392 88.21 kVAr	V = 0.9578 210 kVAr	V = 0.9712 269.95 kVAr
Node 675	V = 0.9392 176.4 kVAr	V = 0.9578 301.1 kVAr	V = 0.9701 417.6 kVAr

Replacing the MSC with a buck cell shows an improvement in the overall voltage profile of the system because of an increase in reactive power generated. The buck cell has higher overall capacitance compared to the MSC. The buck

cell also has a better dynamic response when compared to the MSC. The boost cell provides greater leading reactive VARs in comparison to the buck cell and also provides the same dynamic performance. Improvement in the overall voltage profile of the system with the buck and boost cells is shown in Figure 8.5.

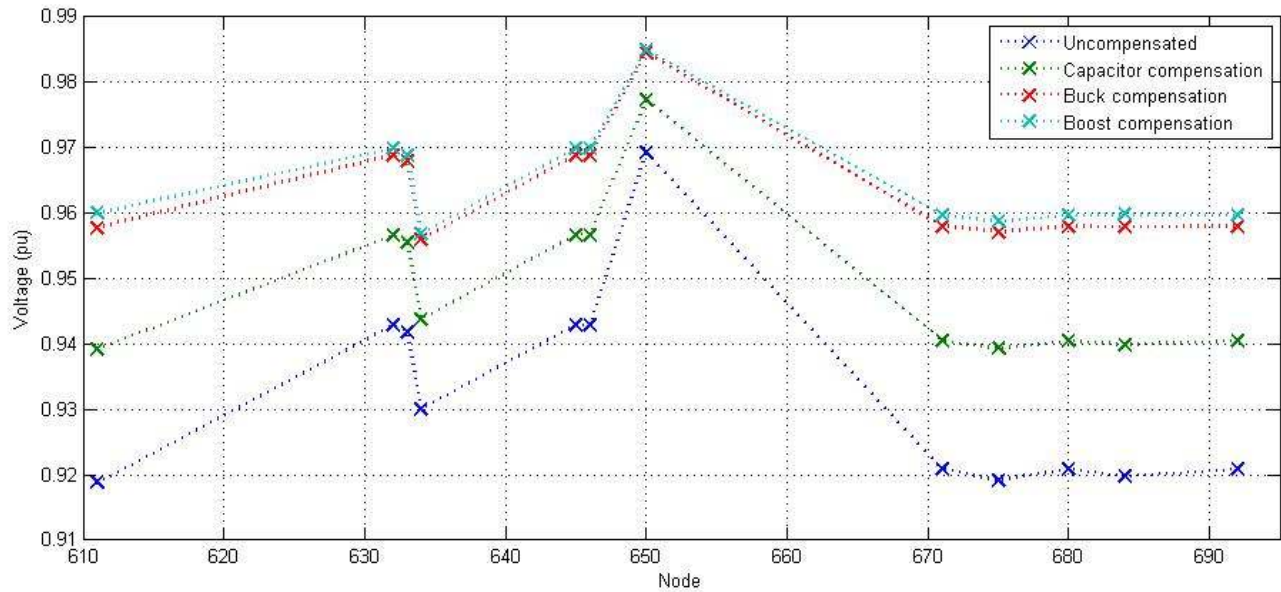
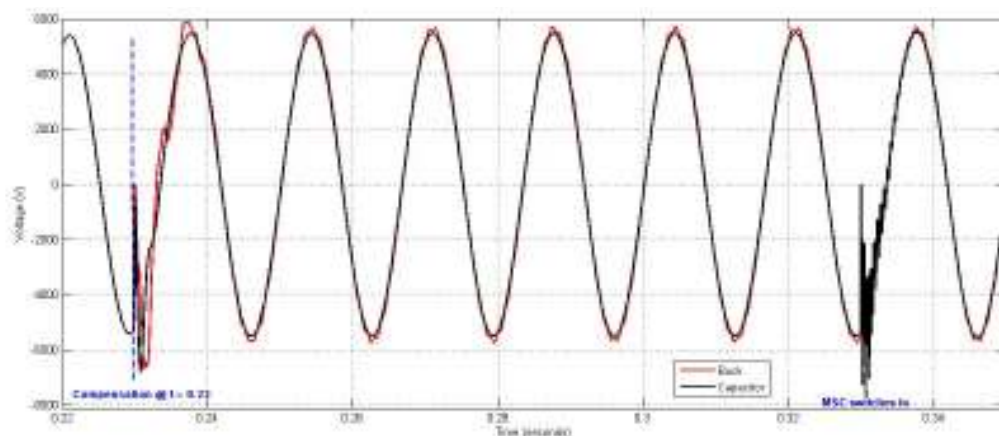
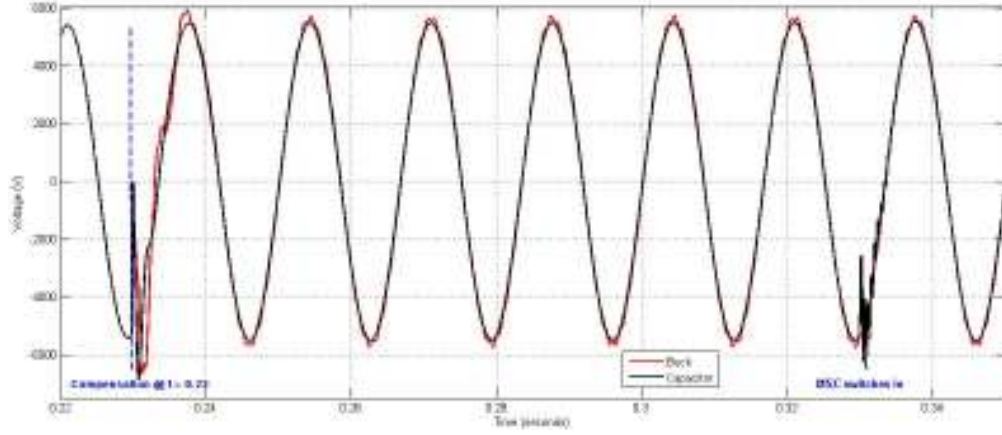


Figure 8.5: Voltage (rms) profile of the IEEE 13 node test feeder with and without compensation.

The improved dynamic response of the voltage is shown in Figure 8.6 and 8.7

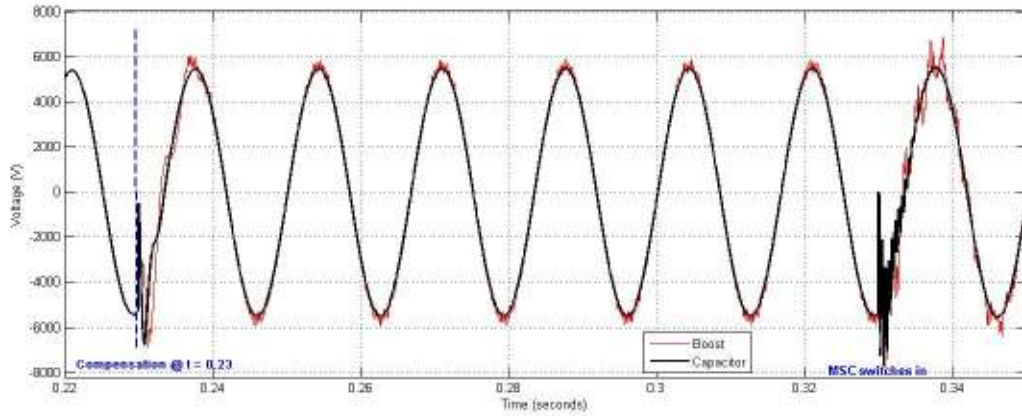


(a)

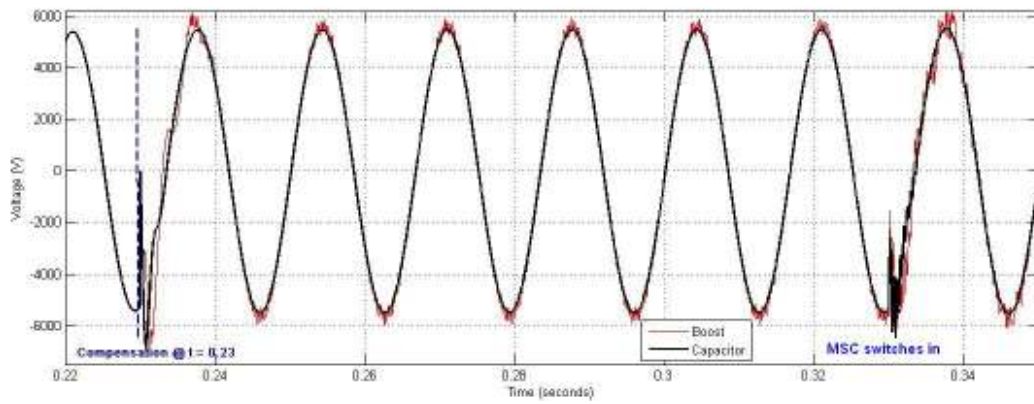


(b)

Figure 8.6: Dynamic response of buck compensators: (a) node 611, (b) node 675.



(a)



(b)

Figure 8.7: Dynamic response of boost compensators: (a) node 611, (b) node 675.

8.3 IEEE 34 NODE TEST FEEDER

The second benchmark system used to study impact of the ILSTATCOM is the IEEE 34 node test feeder. The system is an actual feeder in Arizona, characterized by long line lengths and light loads. Control of the voltage profile is achieved using voltage regulators and VAR compensation capacitors.

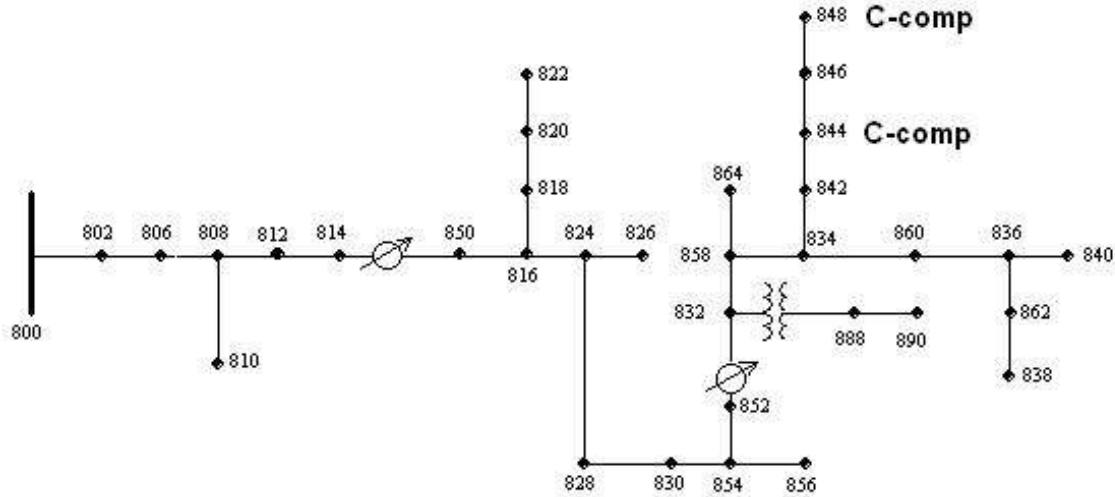


Figure 8.8: IEEE 34 node test feeder

The 34 node test feeder is used as a test system to illustrate the impact of the ILSTACOM when the system voltage drops due to a fault (0.8 pu). Control of the voltage profile on the feeder is achieved using two voltage regulators and two VAR compensation capacitors. Details of the 34 node test feeder system are included in Appendix A.

Improvement in the voltage profile of the system with and the ILSTATCOM buck and boost cells is shown in Figure 8.9. As the test system is characterized by long line lengths, a greater improvement in the voltage at the nodes closer to the points of compensation (844 and 848) can be seen.

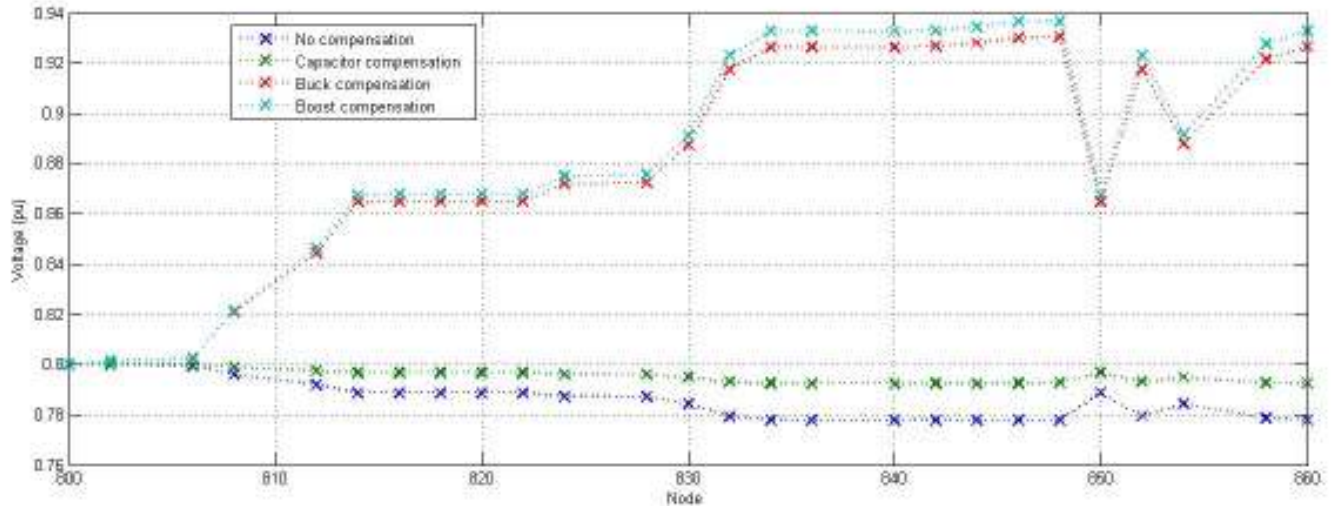


Figure 8.9: Voltage profile with and without compensation

The same dynamic performance of the buck and boost cells is observed in the 34 node test feeder system as seen for the 13 nodes test feeder.

8.4 CONCLUSIONS

Impact of the ILSTATCOM has been studied in the chapter using two standard test systems. The IEEE 13 node and 34 node test feeders have been used to illustrate increased VAR compensation and improved dynamic performance of the ILSTATCOM buck and boost cells compared to conventional VAR compensators (MSC's).

In theory the ILSTATCOM buck cell should generate equal leading reactive VARs as a mechanically switched capacitor. However, the filter capacitor in the converter adds to the VARs, resulting in increased total VARs generated by the buck cell. The boost cells provide more reactive VARs compared to the buck cell. This is because of the effective boost in the voltage across the capacitor as well as the filter capacitor. Results comparing theoretical and simulation results of the buck and boost cells in the 13 node test feeder system has been shown. The second test system illustrates the importance of a distributed reactive power compensator due to the long line lengths. This is evident from the improvement in the voltage profile around nodes 844 – 848.

CHAPTER 9

FAULT ANALYSIS OF A MULTILEVEL DIRECT AC CONVERTER

9.1 INTRODUCTION

An important aspect of the study of multilevel direct AC converters is the reliability and robustness of the converter. This chapter focuses on the study of the different fault modes of the converter. Fault modes considered are simulated to understand the repercussions of each mode and identify the weakest component in each case is.

9.2 DEVICE FAULTS

The topology used in the analysis is the 3-level direct AC converter. The converter has eight AC switches, which corresponds to sixteen single IGBTs, as shown in Figure 9.1. The simulation model considers four-step commutation based on current direction. Component parasitics have also been modeled, as this impacts residual energy etc., during faults.

Failure of a device is the first fault type considered. The faulted IGBT is assumed to fail-short, i.e., failure of the device results in a short circuit across the collector and emitter terminals. There are a large number of combinations that can be considered for device failures. Seven combinations are selected and have been simulated to understand the impact of failure of IGBTs in a multilevel AC converter. Table 9.1 lists the faults considered. Simulation results for each fault are shown together with a table that lists the components affected by the fault.

Simulations consider the converter rated at 100 kVA at 2400V on the input and 2880V on the output, i.e., the converter is operated in the boost mode. It is assumed that all components are rated for a 20% short term overload.

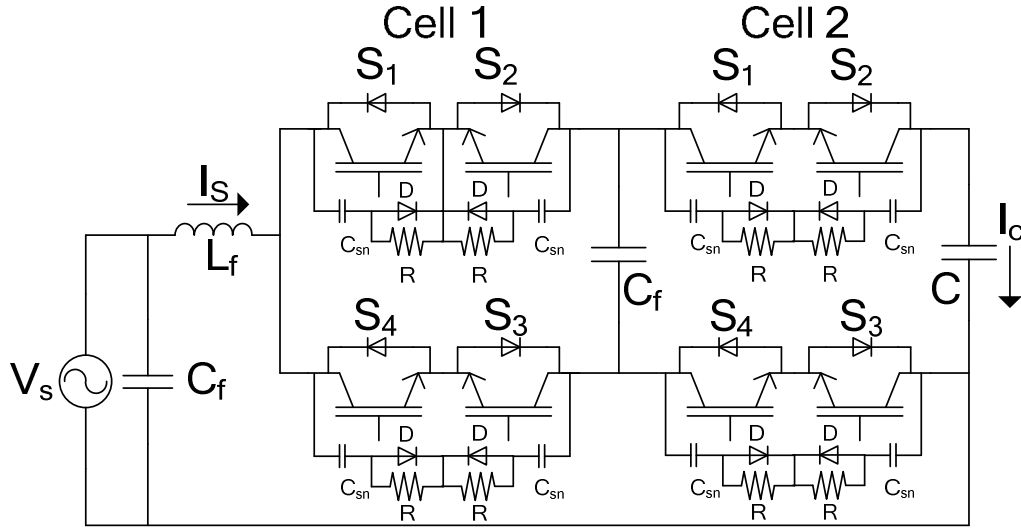


Figure 9.1: 3-level ILSTATCOM boost cell

Table 9.1: Device failures considered

	Cell 1				Cell 2			
Fault	S1	S2	S3	S4	S1	S2	S3	S4
1								
2								
3								
4								
5								
6								
7								

9.2.1 IGBT FAILURE – SHORT CIRCUIT

Failure of a single or multiple devices has a significant impact on converter operation. The three main points that need to be kept in mind while studying each fault are:

- Each IGBT in an AC switch blocks the voltage during one half-cycle of the cell driving voltage.
- The snubber voltages are determined by the cell driving voltage, i.e., $V_{sn} = V_{cell_pk}$.
- Sum of voltages in each cell equal to zero.

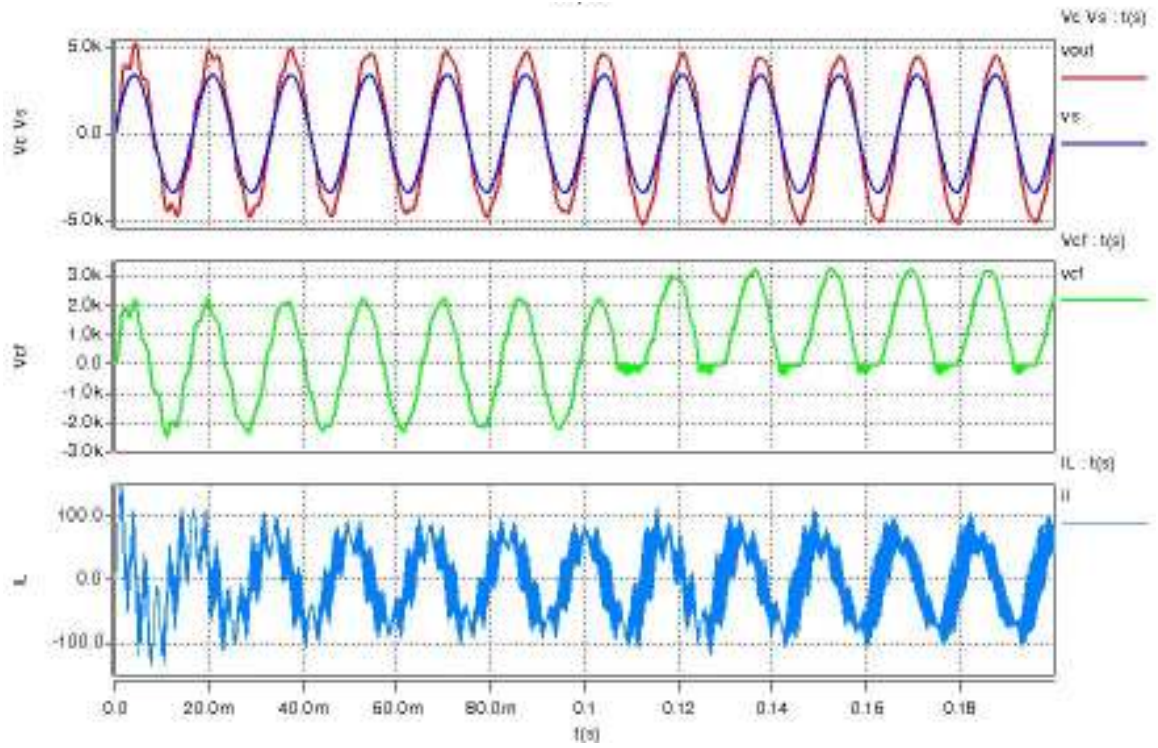
Fault 1 considers failure of a single device, S1 in cell 1. Simulation results for this fault case are shown in Figure 9.2(a) to (g). If device S1 in cell 1 fails the

negative half-cycle of the AC voltage of the voltage across C_f is no longer blocked and no switching takes place during this half-cycle, as shown in Figure 9.2(d). The snubber voltage V_{sn1} causes the voltage V_{cf} to be level-shifted. This results in the voltage V_{sn2} and V_{sn4} to increase to 1.5p.u, as shown in Figure 9.4(d) and (e). The level-shifted V_{cf} implies almost no negative half-cycle; therefore the device S4 in cell 1 blocks a very small voltage, as shown in Figure 9.2(e). Failure of a device in cell 1 impacts the snubber and collector-emitter voltages in cell 2. The level-shifted V_{cf} changes the driving voltage of cell 2, as $V_{cell2} = V_c - V_{cf}$. This results in V_{sn1} and V_{sn3} in cell 2 to increase and V_{sn2} and V_{sn4} to decrease, as shown in Figure 9.4(f) and (g). The voltage V_c remains relatively unchanged.

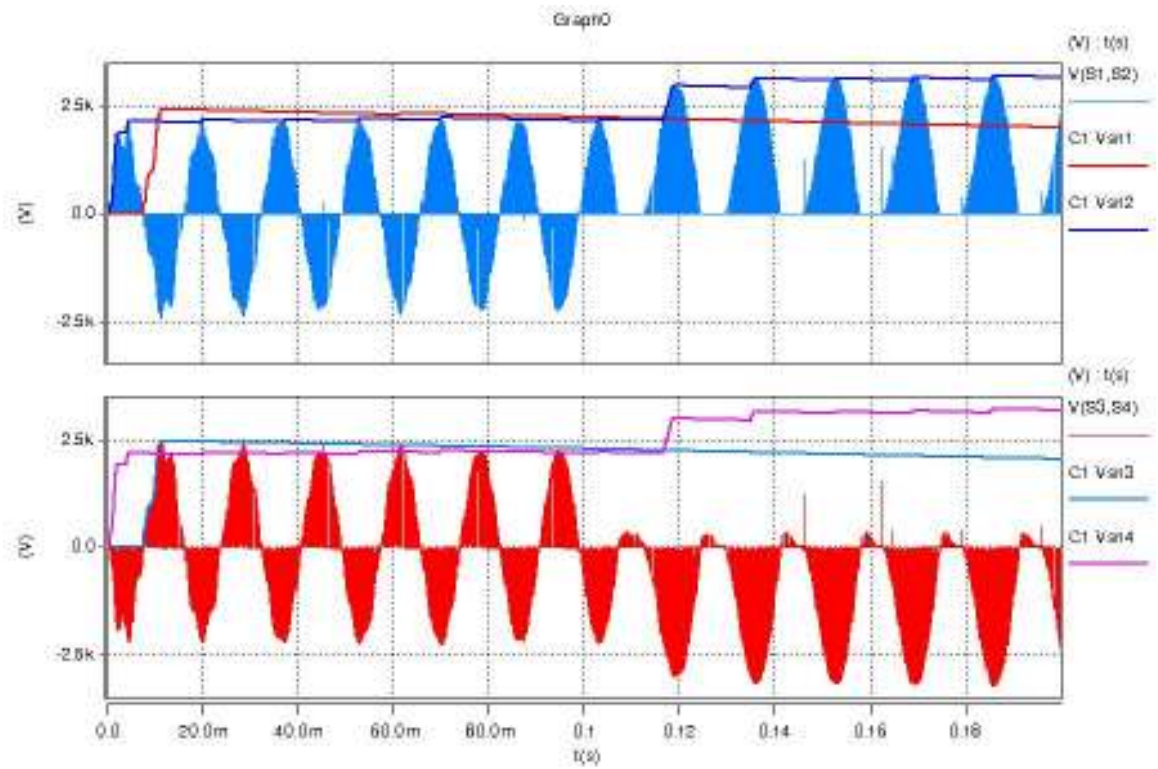
Table 9.2: Component failure– fault 1

Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X		X		X		X
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X		X		X		X	
Passive components							
L				C		Cf	
						X	

(a)



(d)



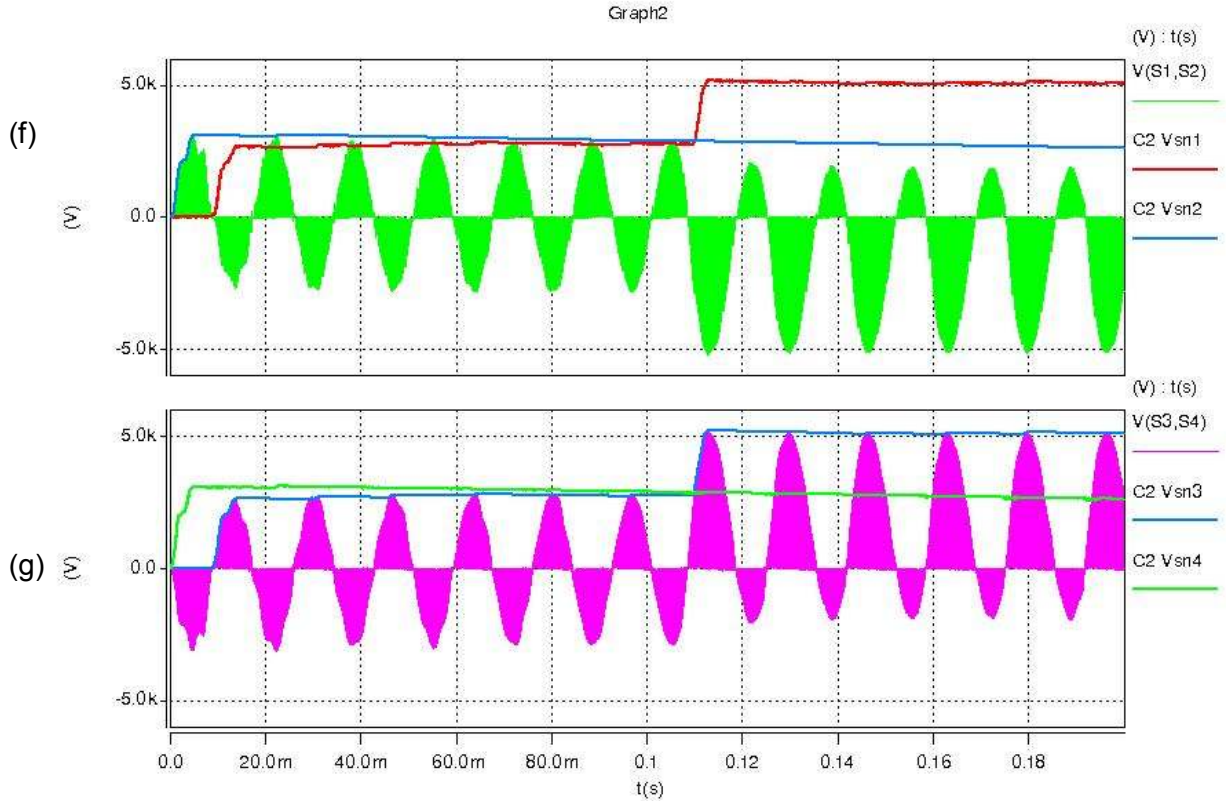


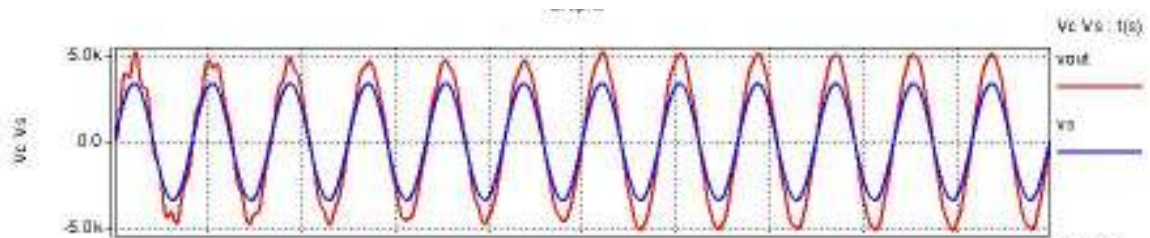
Figure 9.2: Results for fault 1 (a) V_s and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (e) cell 1: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4} , (f) cell 2: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (g) cell 2: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4}

Fault 2 considers failure of devices S1 and S2 in cell 1. This fault causes loss in control of V_{cf} . Applying KVL in cell 1, $V_{cf} = V_{s3} - V_{s4}$, which implies a decrease in the snubber voltages in cell 1, i.e., snubber voltages decay to the value V_{cf_pk} , as shown in Figure 9.3(d) and (e). The value of V_{cf_pk} is determined by the duty cycle of cell 1, in this case $D = 0.833$. The failure of devices S1 and S2 in cell 1 causes the voltage across S3 and S4 to be equal to V_{cf} , as shown in Figure 9.3(b). The change in V_{cf} results in V_c increasing in the both the positive and negative half-cycles causing increased snubber voltages in cell 2, as shown in Figure 9.3(g) and (f). Summary of the components impacted by the fault is given in Table 9.3.

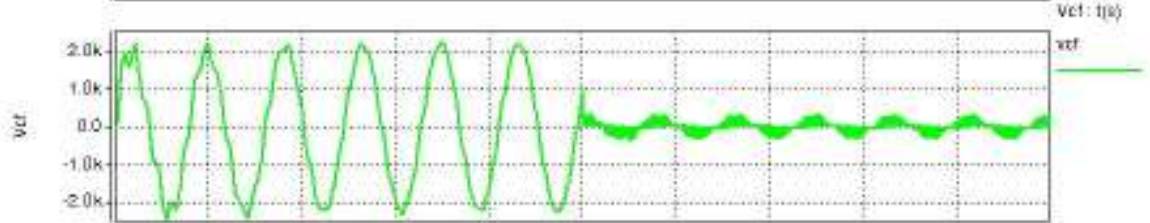
Table 9.3: Component failure– fault 2

Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X						
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X	X	X	X	X
Passive components							
L			C		Cf		
			X				

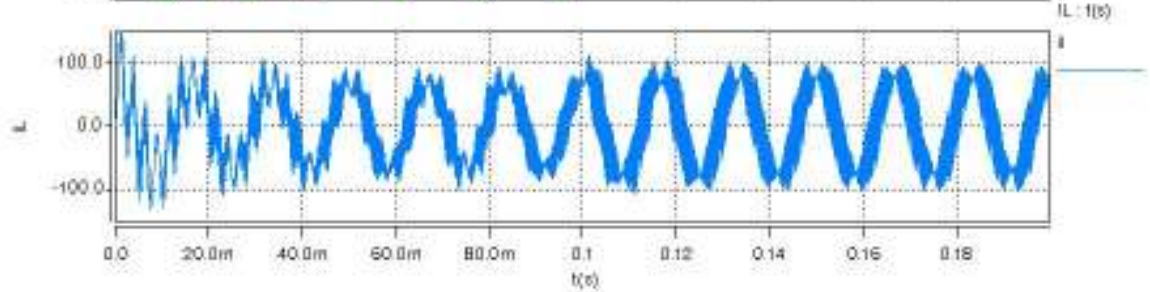
(a)



(b)



(c)



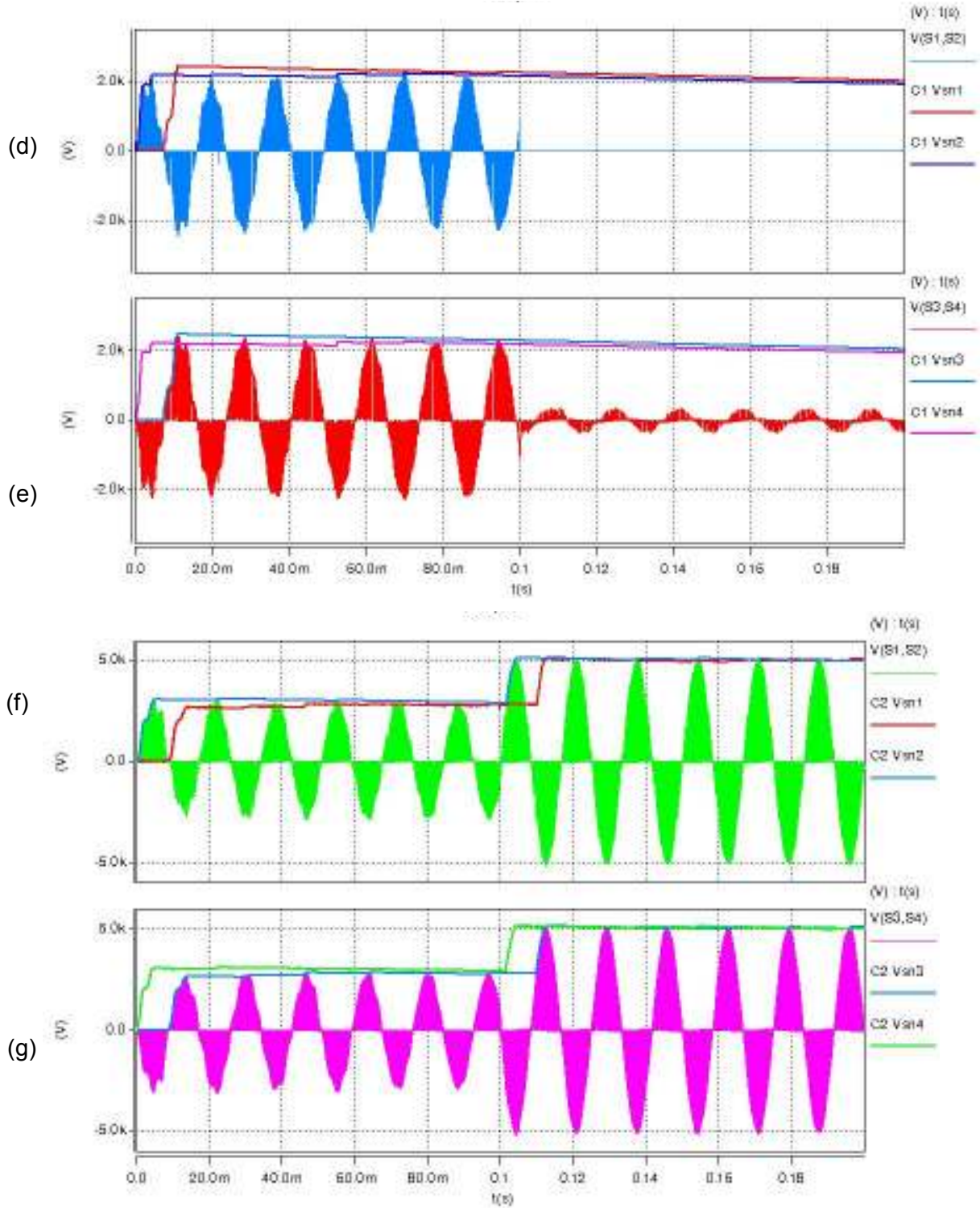
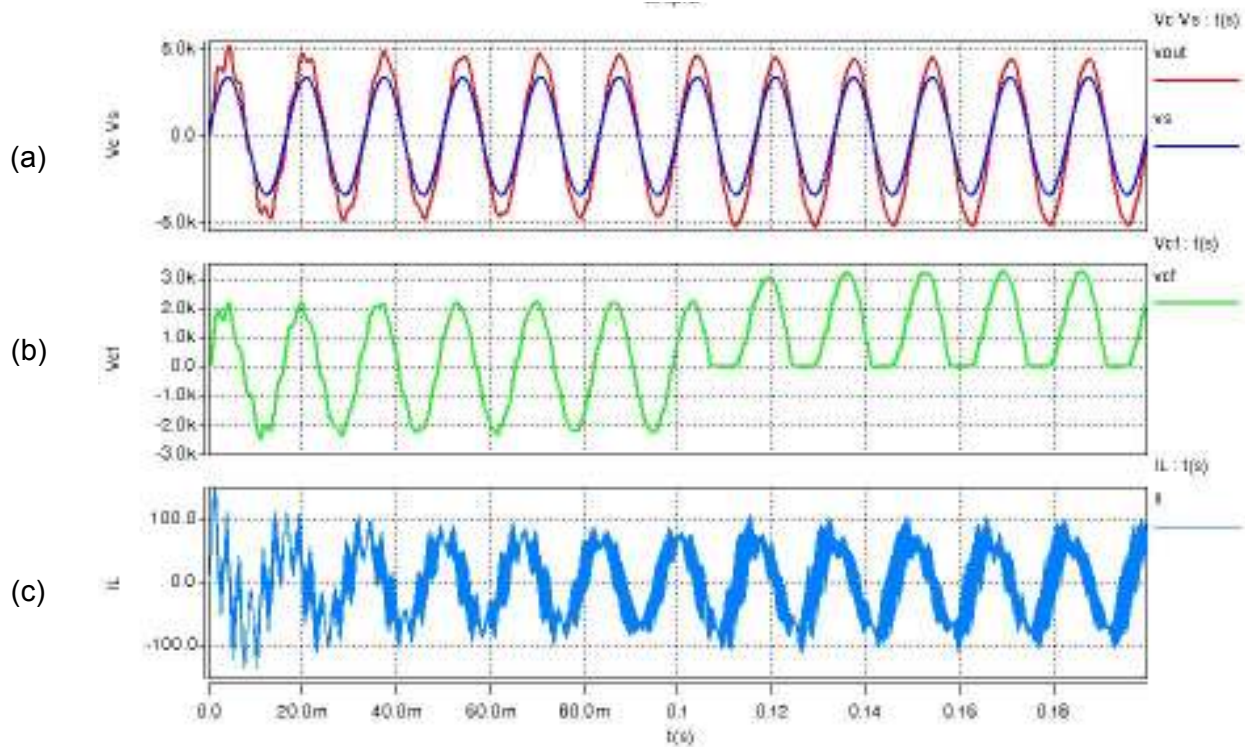


Figure 9.3: Results for fault 2, (a) V_s and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (e) cell 1: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4} , (f) cell 2: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (g) cell 2: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4}

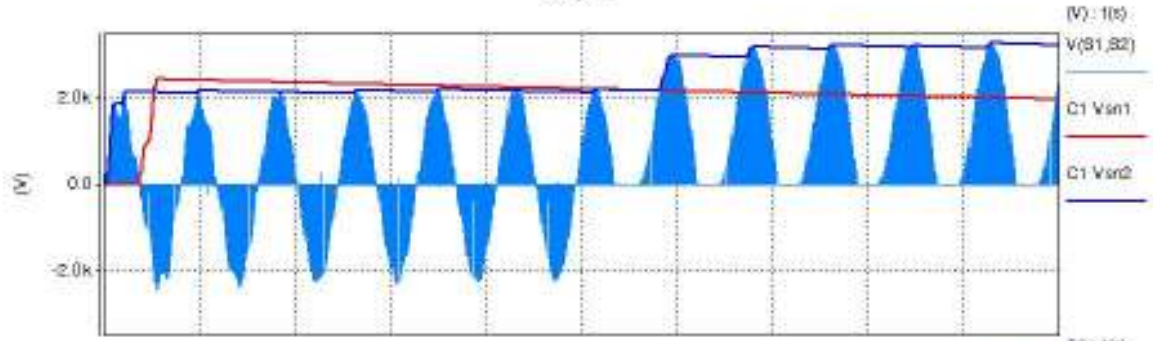
Fault 3 is similar to fault 1. V_{cf} is level-shifted by V_{sn1} . The difference between the two fault modes is the reverse blocking mode for S3 during which device switching is visible (in fault 1). In this case the device is faulted, hence there is no switching. As in the case of fault 1, V_c remains relatively unchanged. The results for fault 3 are shown in Figure 9.4(a) to (f).

Table 9.4: Component failure– fault 3

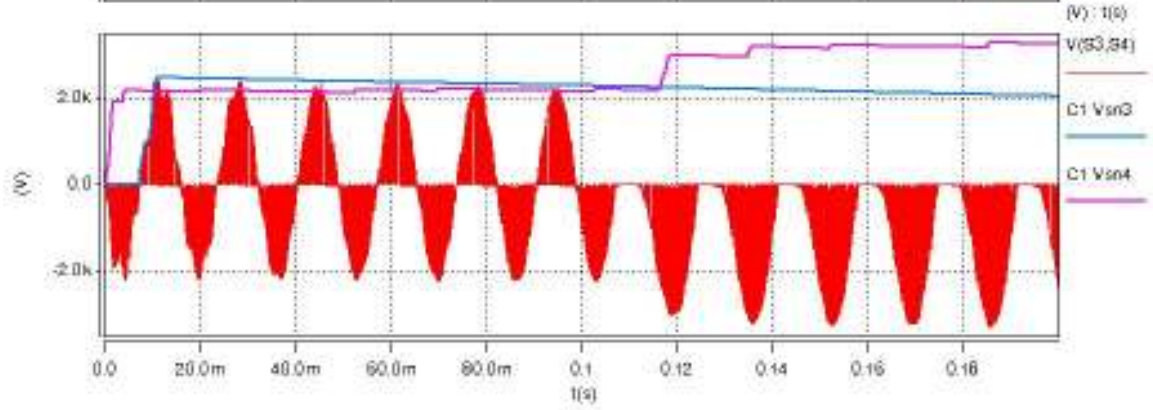
Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X		X		X
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X		X		X		X	
Passive components							
L			C		Cf		
					X		



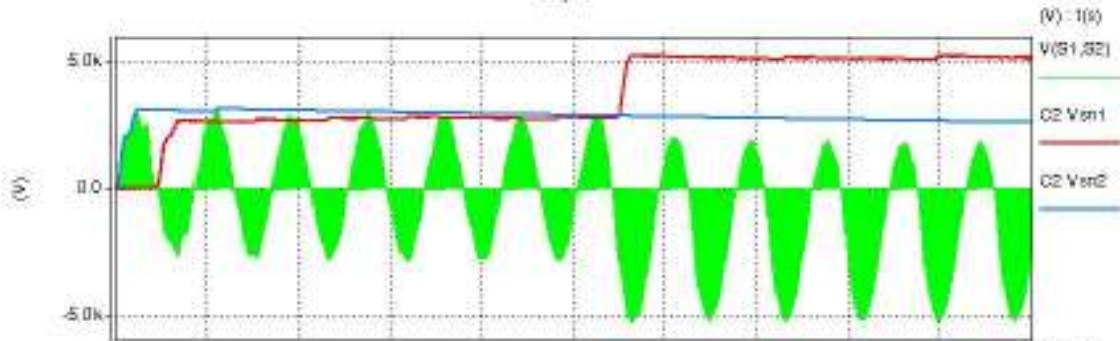
(d)



(e)



(f)



(g)

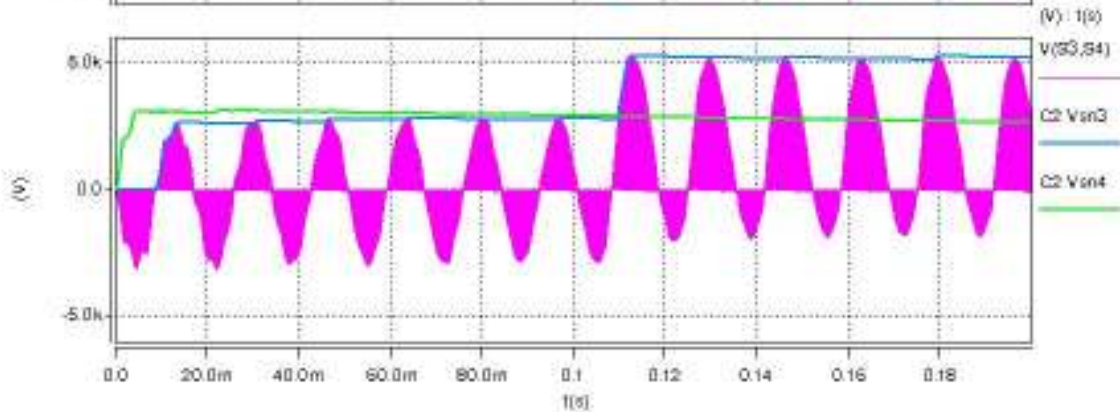


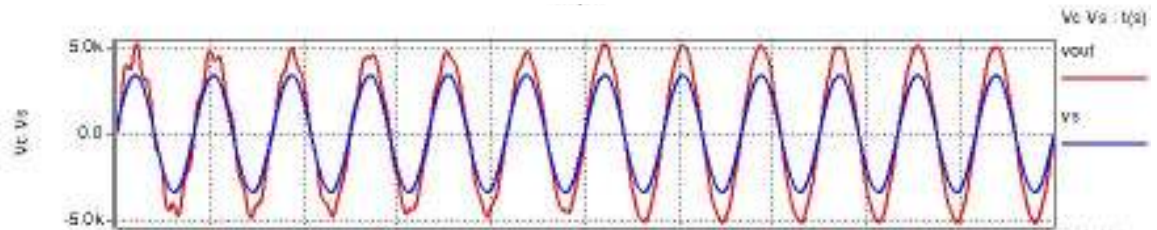
Figure 9.4 Results for fault 3, (a) V_s and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (e) cell 1: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4} , (f) cell 2: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (g) cell 2: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4}

Fault 4 can be explained using fault 2. The failure of S1, S2, and S3 in cell 1 causes the voltage V_{S4} to be impressed across C_f . The magnitude of the voltage is dictated by the amount of time S4 is ON during each switching cycle, i.e., the duty cycle of cell 1.

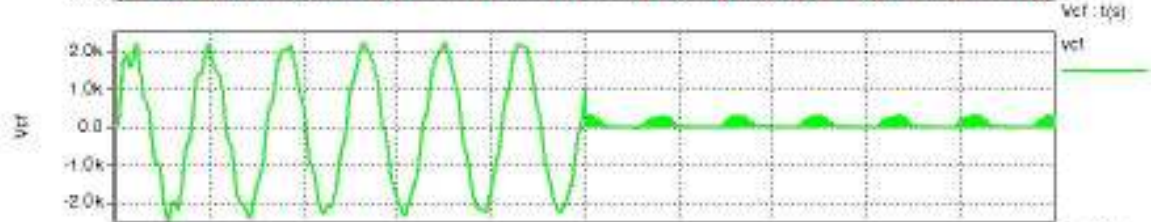
Table 9.5: Component failure– fault 4

Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X					
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X	X	X	X	X
Passive components							
L			C		Cf		
			X				

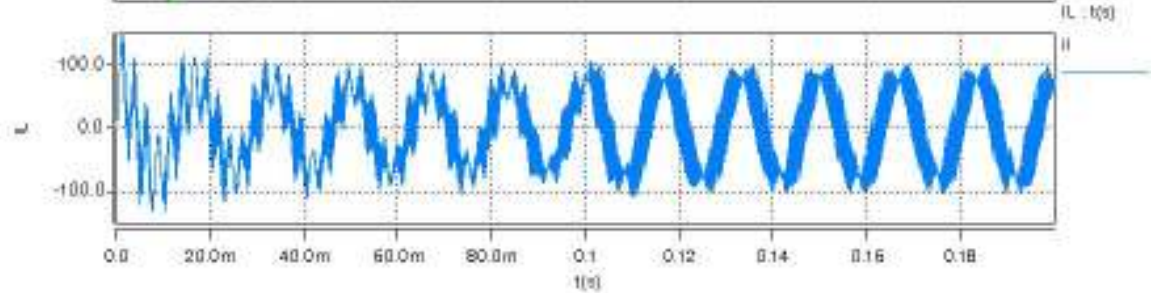
(a)



(b)



(c)



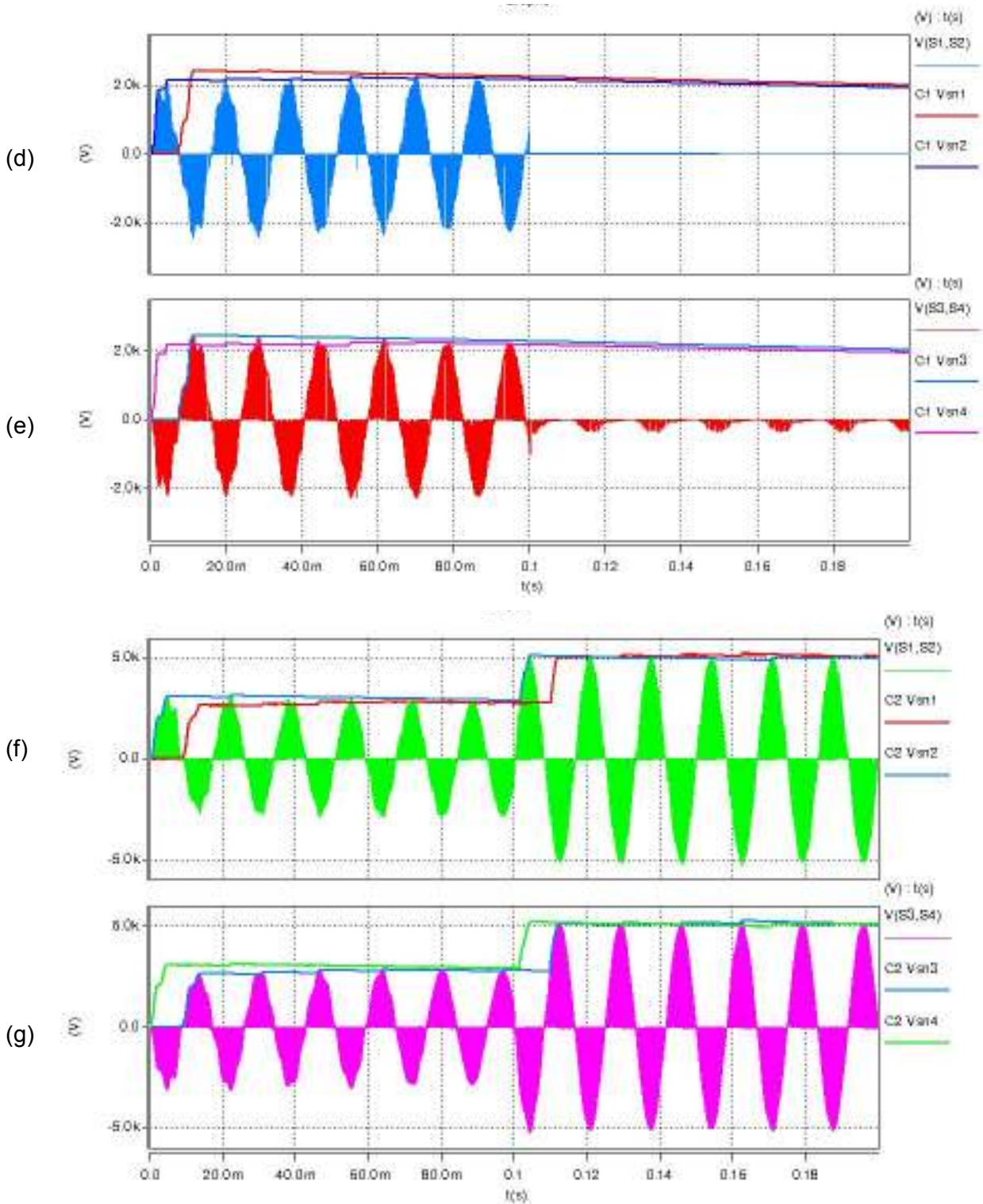


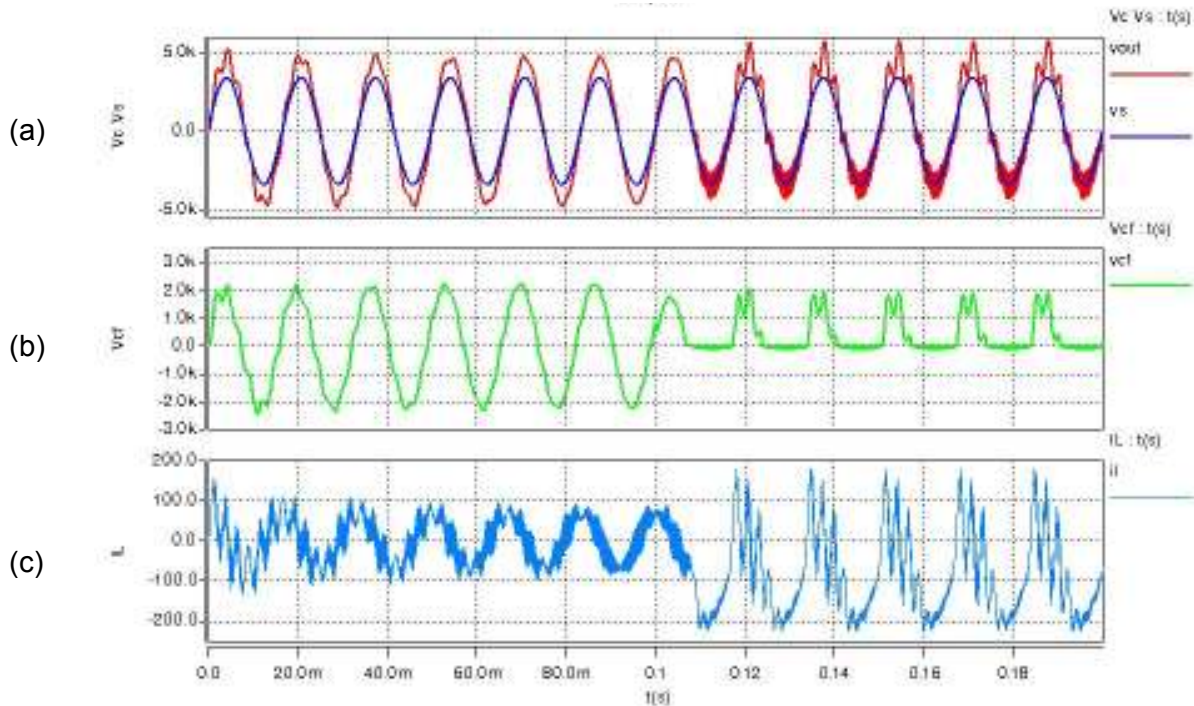
Figure 9.5 Results for fault 4, (a) V_s and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (e) cell 1: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4} , (f) cell 2: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (g) cell 2: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4}

The decrease in V_{cf} , results in an increased cell driving voltage in cell 2. The voltage increases by $\sim 70\%$ of the pre-fault value. This increases the voltage across each IGBT in cell 2, resulting in failure of the devices.

Fault 5 considers a case when IGBTs are faulty in both cells. Simulation results are shown in Figure 9.6. Cell 2 is significantly affected as the voltage $V_{S3,S4}$ increases over the 20% overvoltage threshold, causing device and snubber failure.

Table 9.6: Component failure– fault 5

Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X		X					
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X		X	X	X
Passive components							
L			C		Cf		
X							



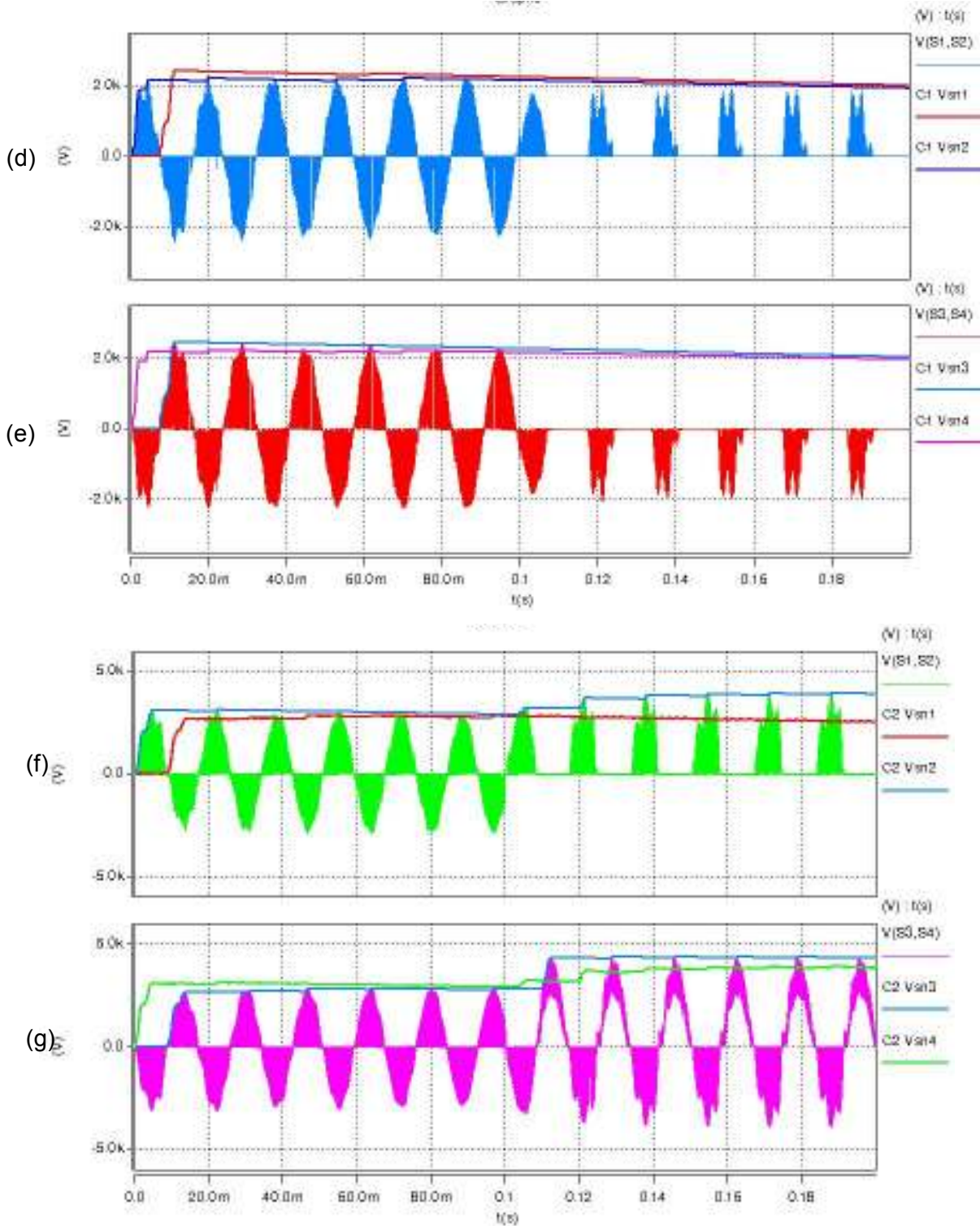
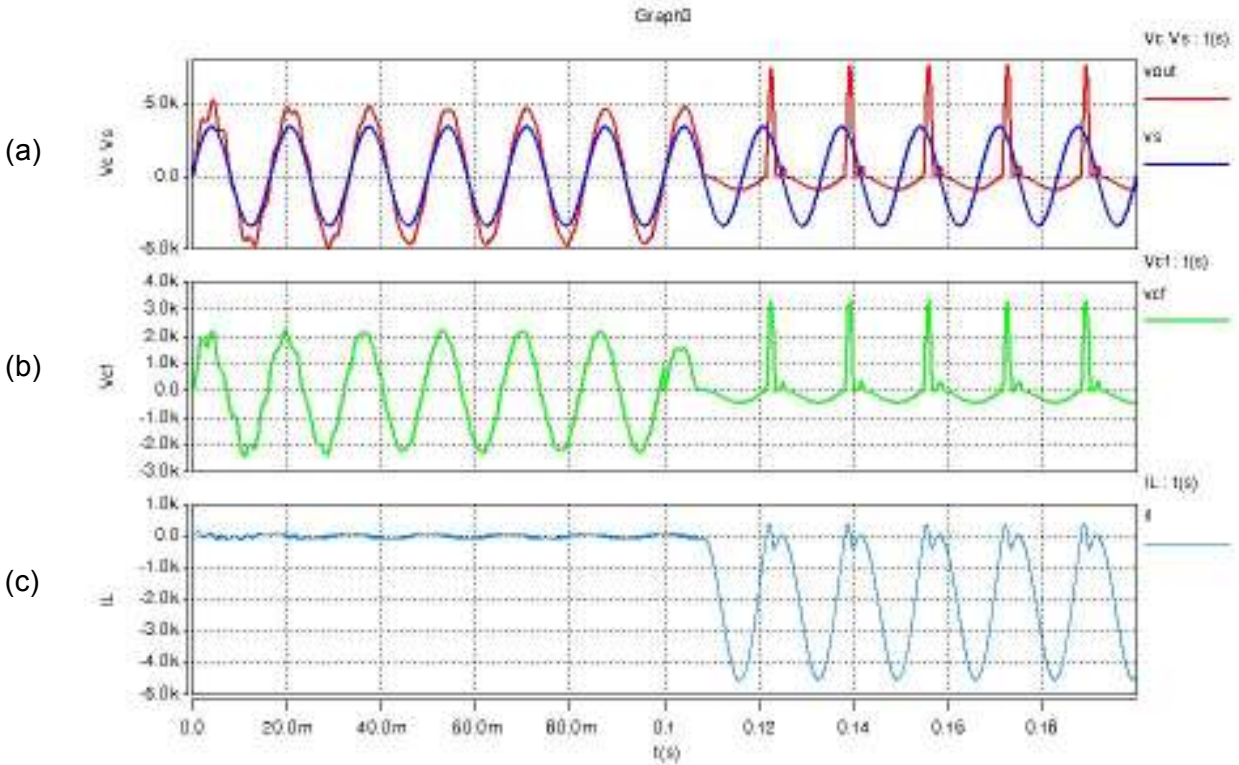


Figure 9.6: Results for fault 5, (a) V_{s1} and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), Vsn1, Vsn2, (e) cell 1: voltage across AC switch (S3, S4), Vsn3, Vsn4, (f) cell 2: voltage across AC switch (S1, S2), Vsn1, Vsn2, (g) cell 2: voltage across AC switch (S3, S4), Vsn3, Vsn4

This fault mode assumes four faulted devices, two in each cell. The impact of this fault is failure of all the components in the converter excluding C_{sn1} and C_{sn3} in cells 1 and 2.

Table 9.7: Component failure– Fault 6

Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X		X		X
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X		X		X
Passive components							
L			C		Cf		
X			X		X		



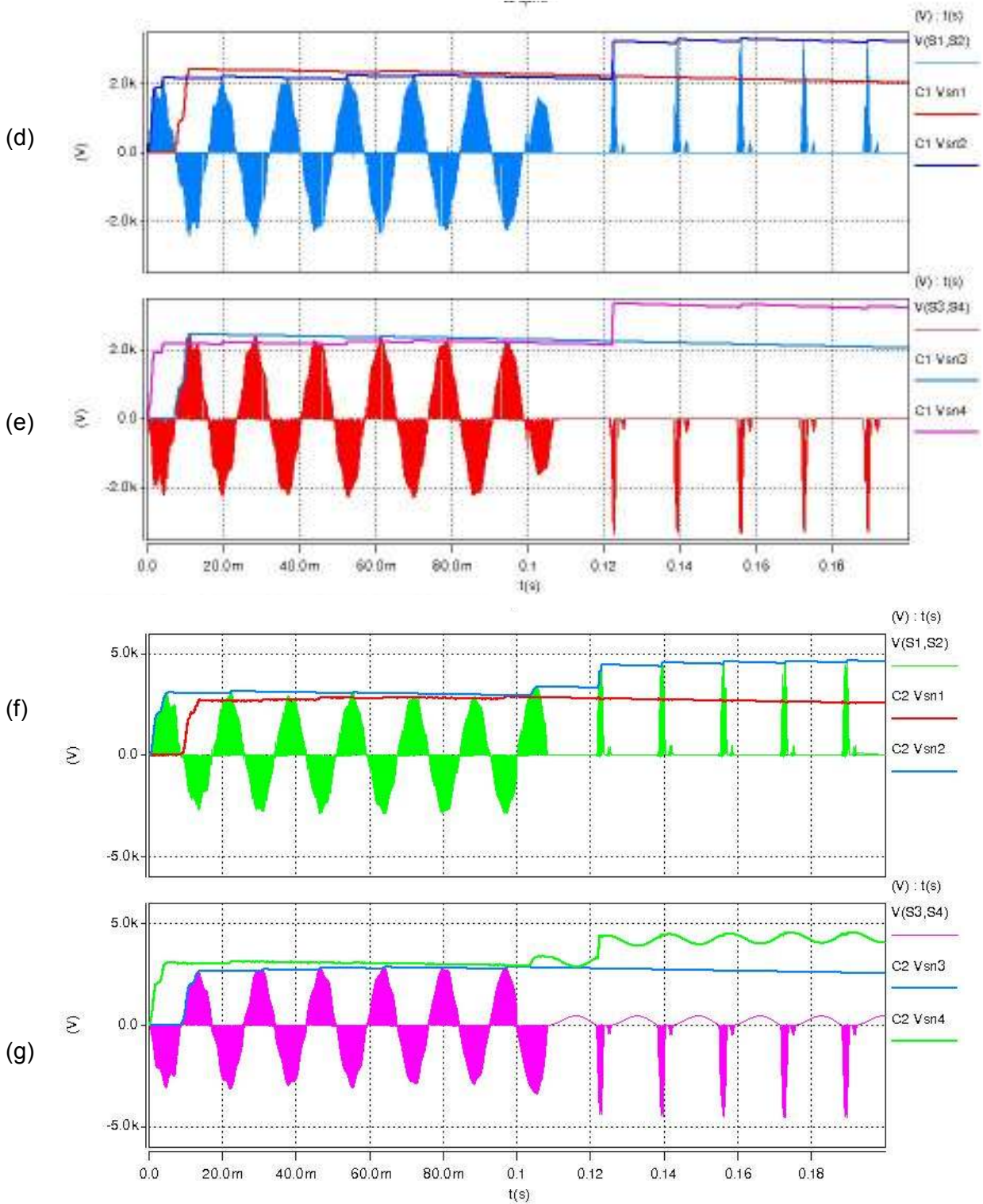
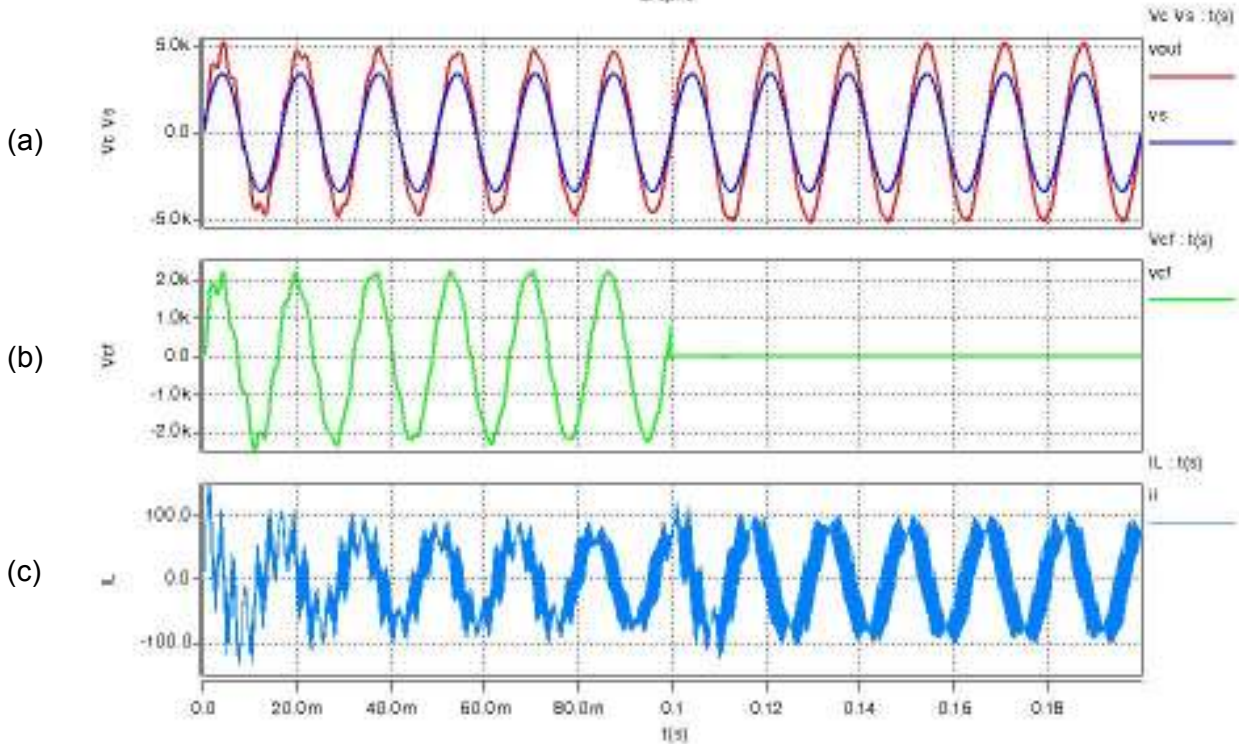


Figure 9.7: Results for fault 6, (a) V_s and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), Vsn1, Vsn2, (e) cell 1: voltage across AC switch (S3, S4), Vsn3, Vsn4, (f) cell 2: voltage across AC switch (S1, S2), Vsn1, Vsn2, (g) cell 2: voltage across AC switch (S3, S4), Vsn3, Vsn4

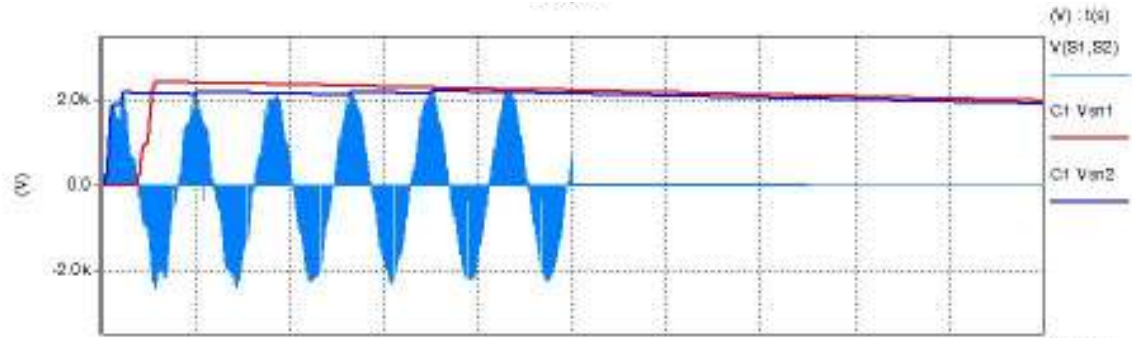
Shorting circuiting of cell 1 is simulated in fault 7. In this case the voltage across all four IGBTs in cell 1 is zero, with the snubber voltages equal and discharging with an RC time constant, T . The driving voltage of cell 2 is twice the pre-fault value, which results in failure of all the IGBTs. The inductor current does not increase significantly; therefore no damage will be caused to L .

Table 9.8: Component failure– fault 7

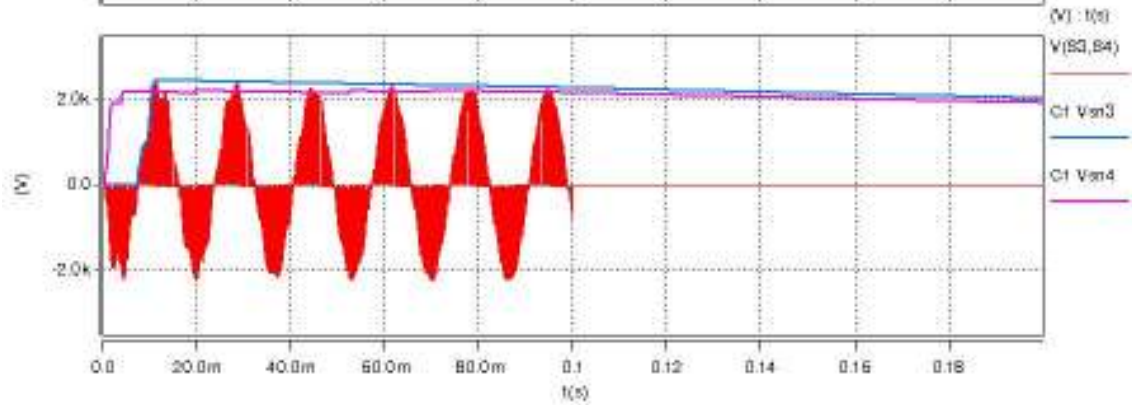
Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X				
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X	X	X	X	X
Passive components							
L				C		Cf	
				X			



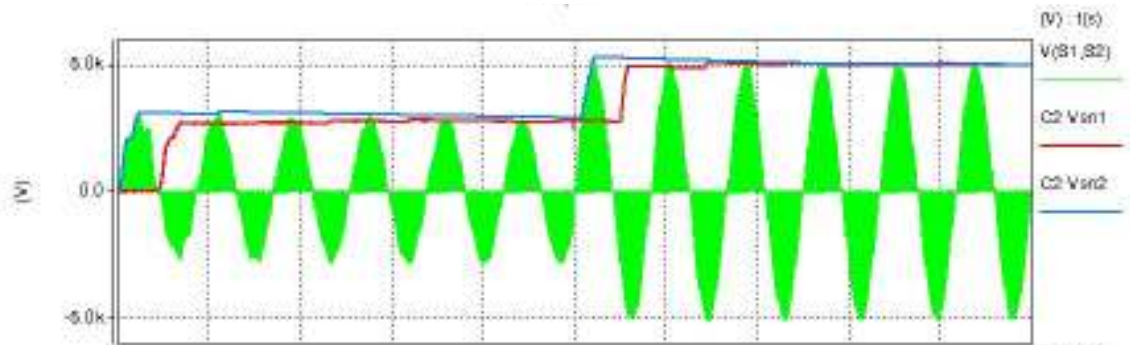
(d)



(e)



(f)



(g)

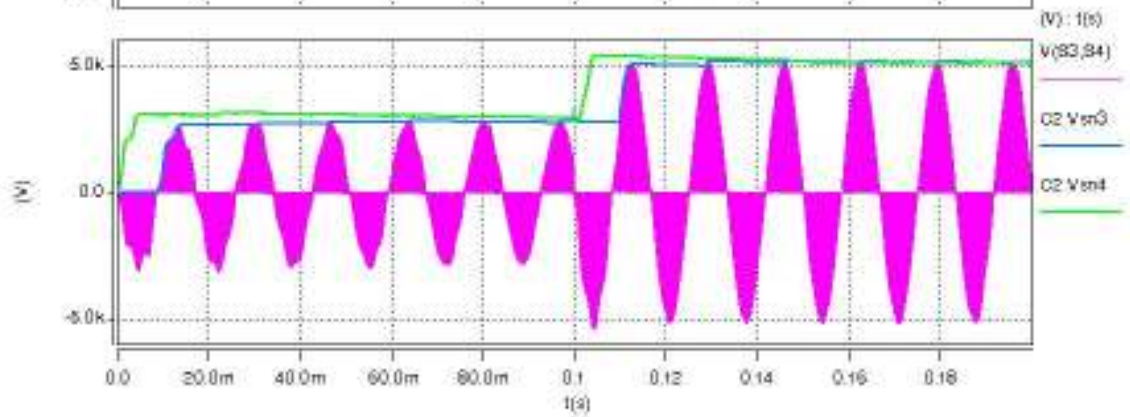


Figure 9.8: Results for fault 7, (a) V_s and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (e) cell 1: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4} , (f) cell 2: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (g) cell 2: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4}

9.3 FAILURE OF PASSIVE COMPONENTS

Failure of passive components in the converter is studied in this section. The two components considered are C_f and L , i.e. filter capacitor and boost inductor. The fault condition is studied using the simulation platform used in the fault analysis discussed in the previous section. Components in the converter that are impacted directly by the failure of passive element are identified and listed.

9.3.1 FAILURE OF C_f

Failure of the filter capacitor is analyzed in this section. The filter capacitor is used to control device stresses. The voltage across the filter capacitor is regulated to a desired value, in this case $V_c/2$, to ensure individual IGBTs have a voltage stress of $V_c/2$.

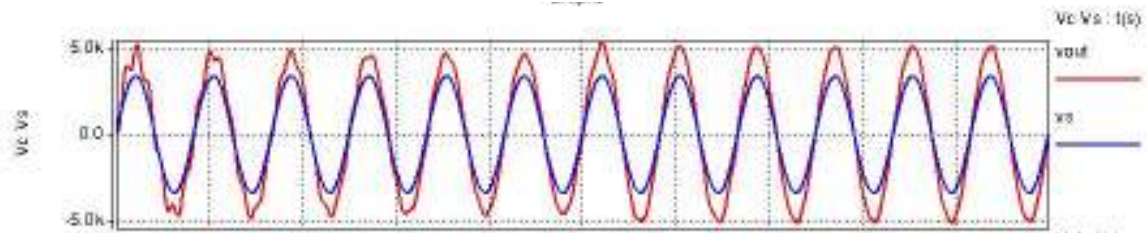
The capacitor is assumed to fail-short. Simulation results illustrating the impact of this fault are shown in Figure 9.9. Table 9.9 lists the converter components that are impacted by this fault.

Table 9.9: Component failure– C_f fault

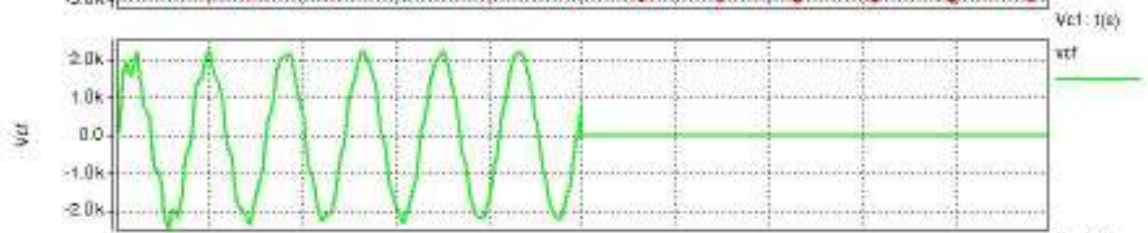
Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
X	X	X	X	X	X	X	X
Passive components							
L				C		Cf	
						X	

Failure of C_f will result in doubling of the cell driving voltage of cell 2. The snubber capacitors in cell 1 discharge over time, and the IGBT's and snubbers in cell 2 see a voltage of V_c . This will result in failure of cell 2 as well. The inductor current does not rise significantly; therefore L will not be affected.

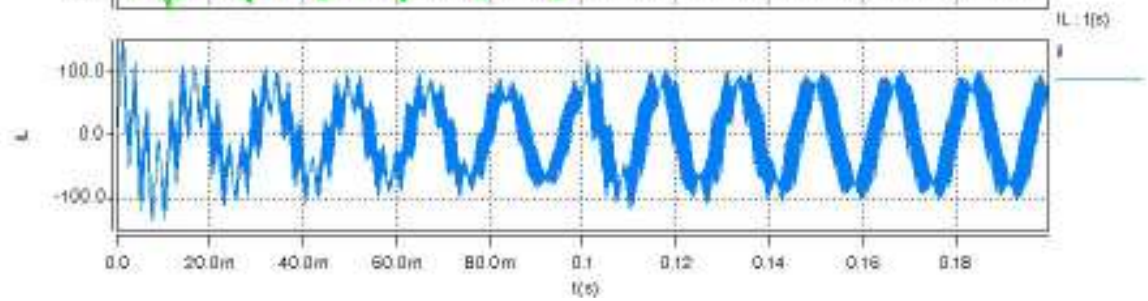
(a)



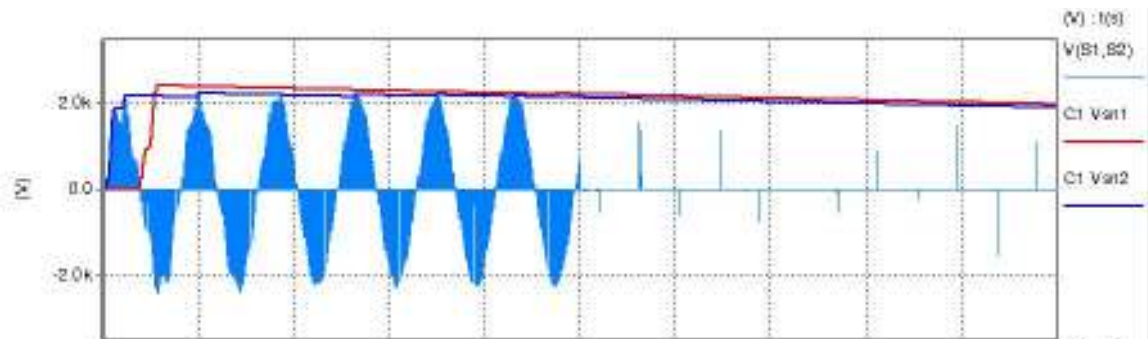
(b)



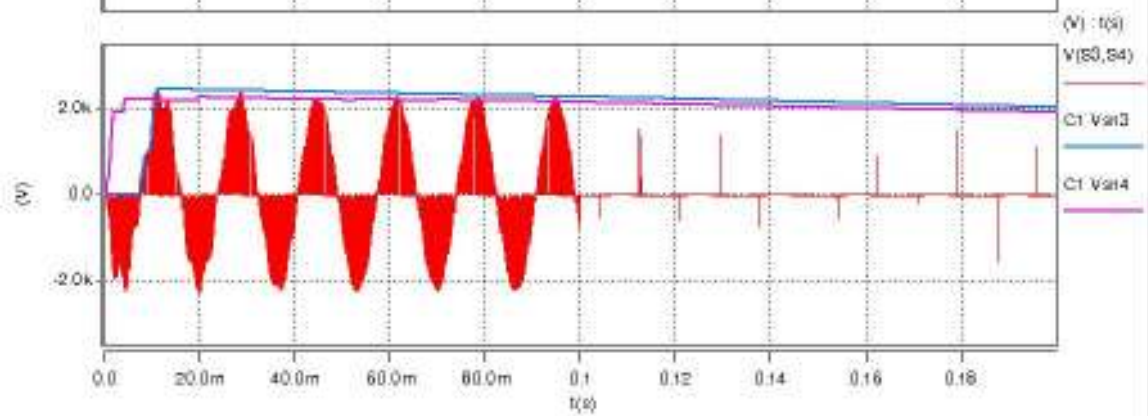
(c)



(d)



(e)



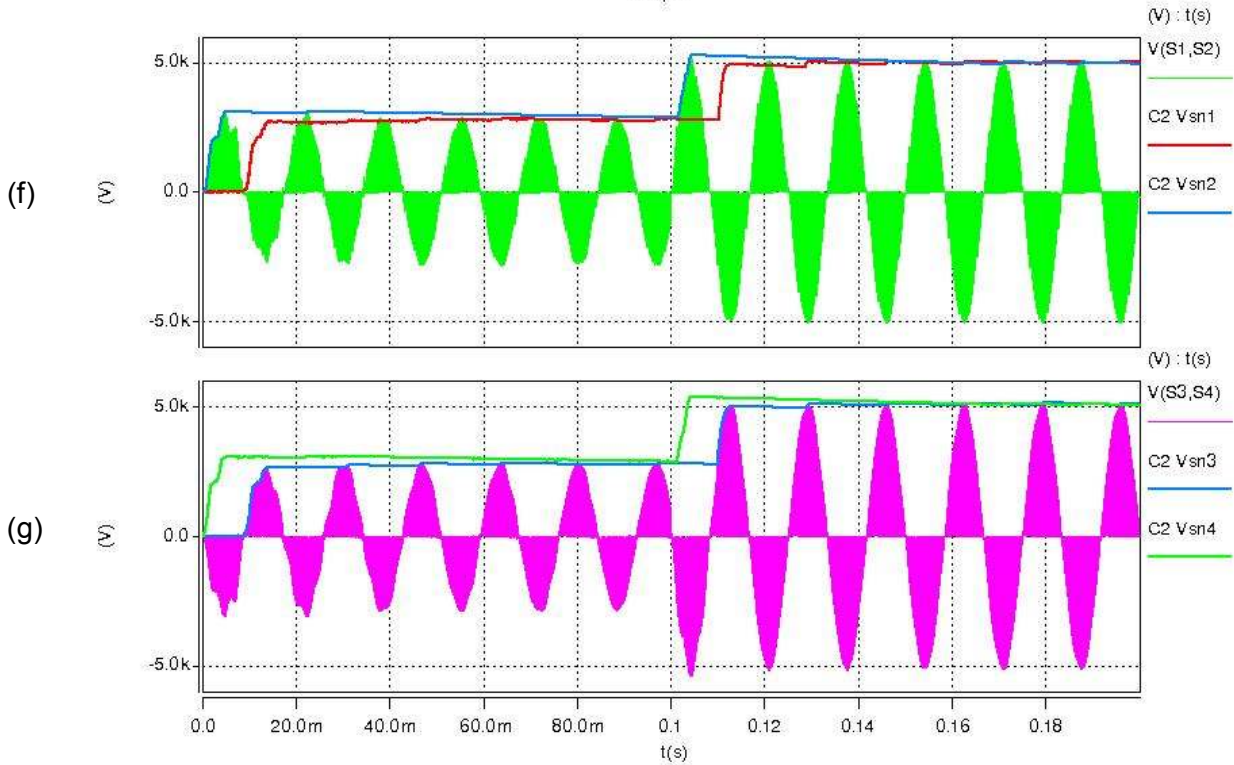


Figure 9.9: Results for C_f fault, (a) V_s and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (e) cell 1: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4} , (f) cell 2: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (g) cell 2: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4}

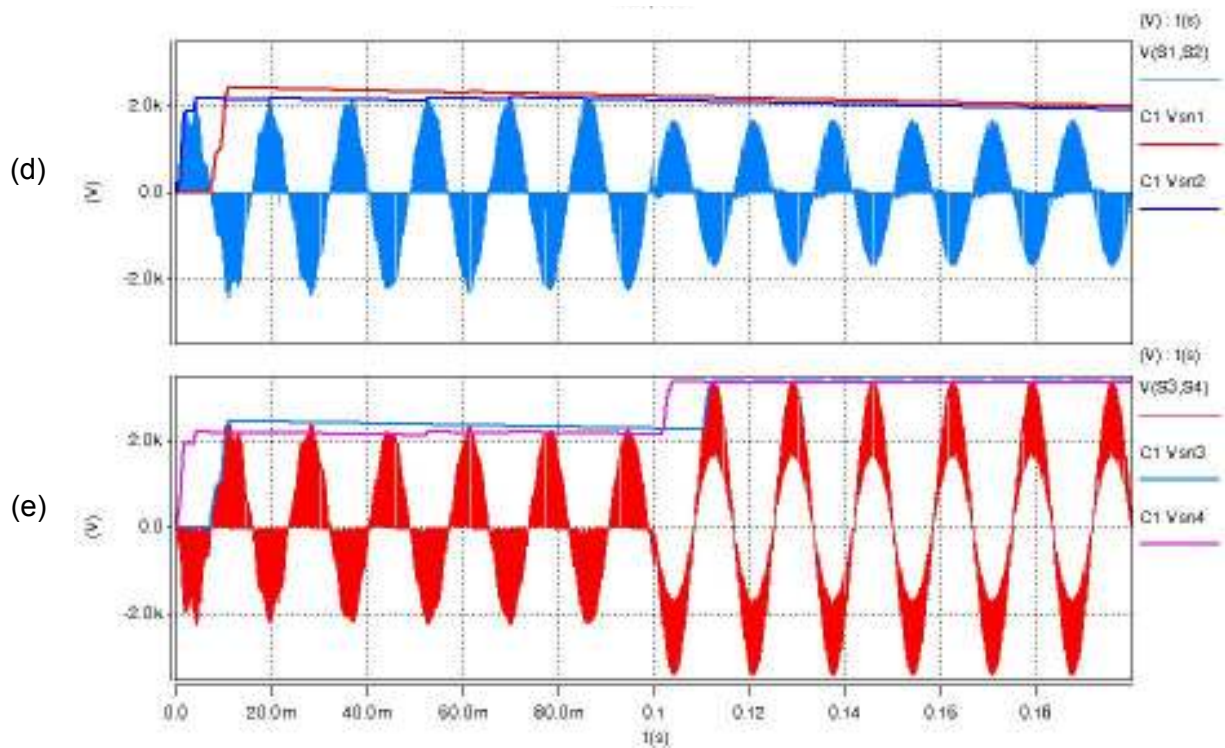
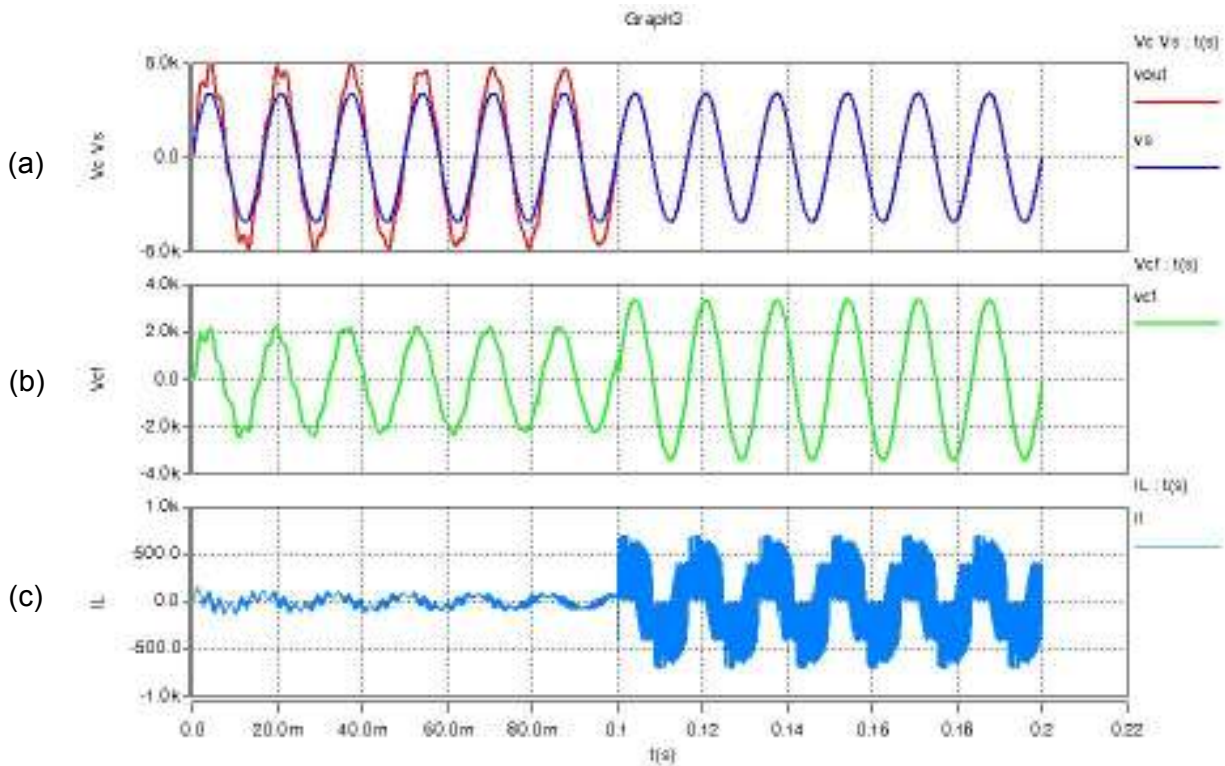
9.3.2 FAILURE OF L

Failure of the boost inductor is considered in this section. The passive component is assumed to fail-short. Figure 9.10 illustrates the impact of this fault condition.

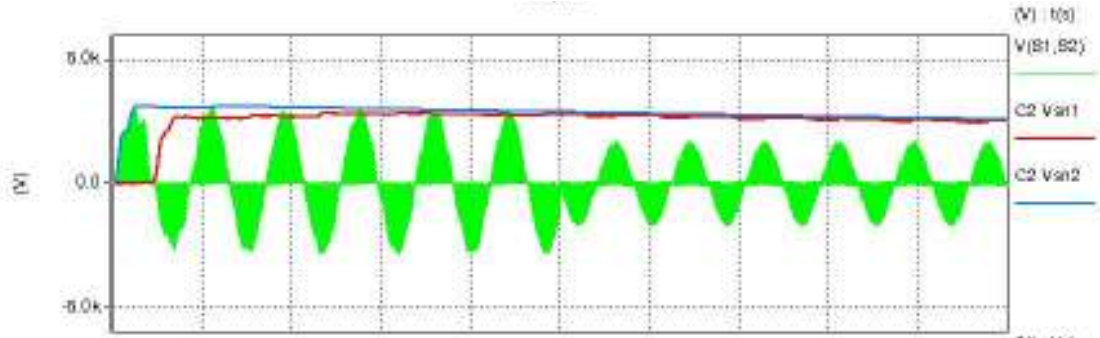
Table 9.9: Component failure– L fault

Cell 1							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
		X	X			X	X
Cell 2							
IGBT1	IGBT2	IGBT3	IGBT4	Csn1	Csn2	Csn3	Csn4
Passive components							

L	C	Cf
X		



(f)



(g)

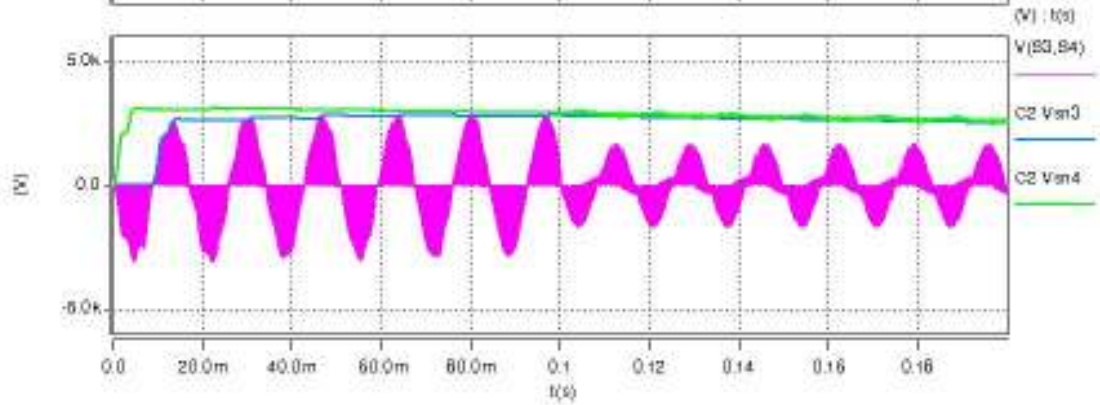


Figure 9.10: Results for L fault, (a) V_s and V_{out} , (b) V_{cf} , (c) I_L , (d) cell 1: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (e) cell 1: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4} , (f) cell 2: voltage across AC switch (S1, S2), V_{sn1} , V_{sn2} , (g) cell 2: voltage across AC switch (S3, S4), V_{sn3} , V_{sn4}

Failure of the inductor will cause V_c to be equal to V_s . This will result in a decreased output voltage. The current will increase significantly causing V_{cf} to increase as well. The components significantly affected in this fault mode are the devices S3, S4 and corresponding snubbers in cell 1. The increased current will probably damage all the components in the circuit; this is not reflected in Table 9.9.

9.4 CONCLUSIONS

This chapter focuses on understanding the fault modes in a multilevel converter. There are a large number of fault types and combinations of fault modes that can be considered, a few have been selected. The multilevel converter is a cascaded structure. It is therefore important to understand impact of the failure of various components in the converter. Each fault type is

simulated and the affected components listed. This information provides insight into the safety margins and protection methods required for the converter.

CHAPTER 10

DESIGN AND IMPLEMENTATION OF A MEDIUM VOLTAGE ILSTATCOM BOOST CELL

10.1 INTRODUCTION

The design and implementation of a medium voltage prototype of the ILSTATCOM is presented in this chapter. The design process encompasses the following:

1. Selection of voltage and power ratings.
2. Selection of the type of cell (buck/boost) and number of levels of the converter.
3. Electrical design of each component
4. Mechanical design of the converter
5. Thermal design of the converter

Each component is designed and characterized to understand individual component characteristics. Based on the characteristics of each component the overall converter design is modified. Thermal analysis for the converter is studied and comparisons to conventional voltage source based converters are made to facilitate a deeper understanding of the thermal limitations of direct AC-AC based converters verses DC-AC converters. Complexities with implementation are detailed to the extent necessary. Issues with commutation modes, snubber implementation and specific fault modes encountered during testing are discussed. Finally, illustrations of the experimental setup with experimental results are shown.

10.2 TECHNICAL SPECIFICATIONS

The topology, voltage, and power levels have been selected to allow for a deeper understanding of the issues and challenges with scaling the

ILSTATCOM. Further, it is desirable to test boost operation of the converter so as to illustrate STATCOM mode of operation, i.e., increased reactive VAR support under reduced line voltage conditions. Therefore, as a first step the topology of the prototype (buck or boost cell) is to be decided, followed by details of the technical specification i.e., the operating voltage and power levels. The following steps are carried out in the design process.

1. Selection of the operating voltage and power levels.
2. Determine topology for medium voltage prototype of the ILSTATCOM.
This step involves selection of either a buck or boost cell.
3. Determine the number of levels of the converter. The operating voltage dictates the number of levels in the multilevel ILSTATCOM.
The factors that influence the choice of voltage and power levels are:
 - i. Cost effectiveness of the solution
 - ii. Trade-off between conditions that can be tested in a laboratory environment and realistic voltage levels in distribution systems.
 - iii. Availability of long lead time components such as IGBTs, heat sinks, and capacitors.
4. Electrical design of each component
 - i. Theoretical design
 - ii. Component characterization
5. Mechanical design of the converter

The operating voltage and power levels selected for the laboratory prototype are shown in Table 1.1. The ILSTATCOM will be designed to provide VAR support of **100 KVAR @ 2.4 kV**.

Table 10.1: Ratings for the medium voltage prototype

Power	100 kVAR
AC nominal voltage	4.16 kV
Switching frequency	1 – 7 kHz
Overload	20 % short duration

The topology selected for the laboratory prototype is a boost cell. This is primarily to demonstrate the ability of the boost cell ILSTATCOM to generate increased leading reactive VARs under reduced line voltages.

Designing a converter with an operating voltage of 2400V (L-N) requires single IGBTs that can handle voltages up to 3.3 kV peak with switching frequencies between 1 to 7 kHz. Commercially available IGBTs can handle voltages of 1700V, 3300V and 6600V. For a 2.4 kV system, the 6600 V devices would be suitable; however these devices can be switched at frequencies in the range of hundreds of Hz. Scaling to the desired voltage of 2400V can be achieved by using a multilevel direct AC converter shown in Figure 10.1. One possible method to scale to 2.4 kV is using a 3-level direct AC converter to realize an ILSTATCOM boost cell. This requires each device to be rated for 0.5pu compared to 1.0 pu (assuming no safety margin).

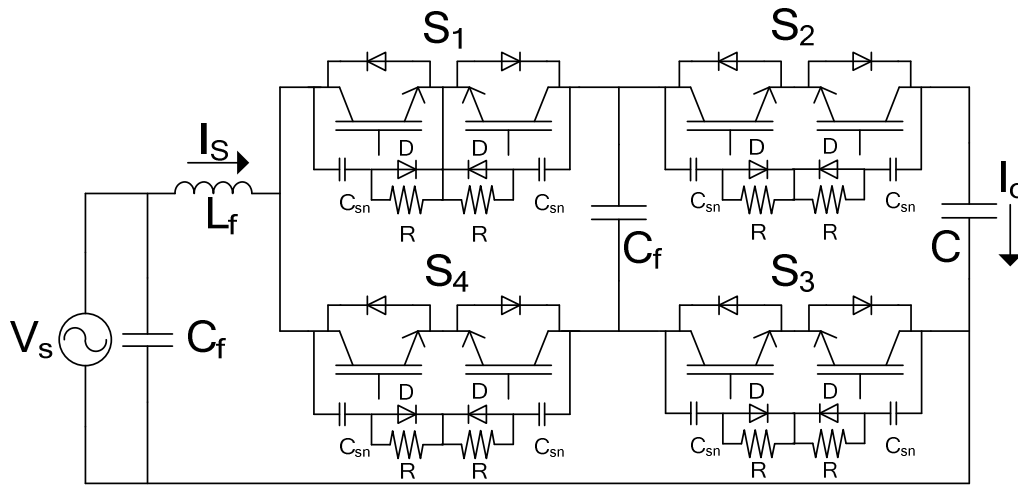


Figure 10.1: 3-level ILSTATCOM boost cell

The major components to be designed for the ILSTATCOM are listed in Table 10.2. The components listed in Table 10.2 correspond to Figure 10.1.

Table 10.2: List of components and ratings

S. No.	Component	Description
1.	V_s	Input voltage source
2.	C_f	Input filter capacitor
3.	L_f	Boost inductor
4.	S1, S1, S3, S4	Common emitter IGBT AC switch
5.	C	Shunt VAR capacitor
6.	R, C_{sn} , D	Snubber resistor, snubber capacitor, and snubber diode

10.3 DESIGN OF 3-LEVEL ILSTATCOM BOOST CELL

The following section details the design and selection of components used in the ILSTATCOM prototype. The final list is shown in Table 10.2. The design of each individual component and justification for selection of the final component (as listed in Table 10.2) will be presented in later sections.

Table 10.3: List of components and ratings

COMPONENT	VALUE/RATING	MANUFACTURER	MAXIMUM OPERATING CONDITIONS
BOOST INDUCTOR	$L = 990 \mu\text{H}$	MICROMETALS POWDER CORE (-2 MATERIAL)	$2400V_{\text{rms}}$, $50A_{\text{rms}}$
FILTER CAPACITOR	$C_F = 5 \mu\text{F}$	$11.7 \mu\text{F} = 3 \times 35\mu\text{F}$, $900V_{\text{rms}}$	$2040 V_{\text{pk}}$ (AC) $2120 V_{\text{rms}}/ 2998 V_{\text{pk}}$ $2700 V_{\text{rms}}/ 3820 V_{\text{pk}}$
SHUNT VAR CAPACITOR	$C = 47 \mu\text{F}$	WESTINGHOUSE 3-PH 300 kVAR, 4160V	$4080 V_{\text{pk}}$ (AC)
SNUBBER CAPACITOR	$C_{sn} = 0.5 \mu\text{F}$ $2 \times 1 \mu\text{F}$, $2000V_{\text{dc}}$	ILLINOIS CAPACITORS	$2040 V_{\text{pk}}$ (DC) (4000 V)
SNUBBER RESISTOR	$R_{sn} = 340 \text{ k}\Omega$	$\frac{1}{2} \text{ W}$ METAL FILM	
SNUBBER	$3 \times 1200\text{V}$, 20A	VISHAY SEMICONDUCTOR	$2040 V_{\text{pk}}$

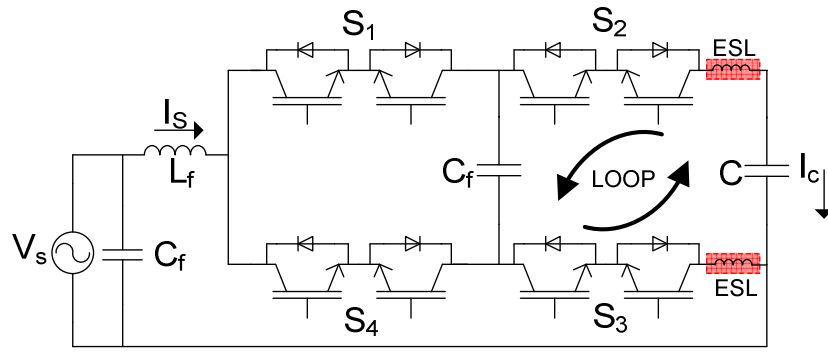
DIODES			(3600 V)
NOMEX INSULATION	20 mil, 6kV insulation	EIS	2.4 kV
KAPTON SHEETS	1 mil, 6kV insulation	AMERICAN DURAFILM	2.4 kV
COPPER SHEETS	10 mil	BASIC COPPER	55A _{rms}
VOLTAGE SENSORS	3000V _{rms} (0 – 4500V _{rms})	LEM	2880 V _{rms}
CURRENT SENSORS	50A _{rms} (0 – 150A _{rms})	LEM	50A _{rms}
MOV'S	2400V	PANASONIC	3X1100V

10.3.1 SHUNT VAR CAPACITOR

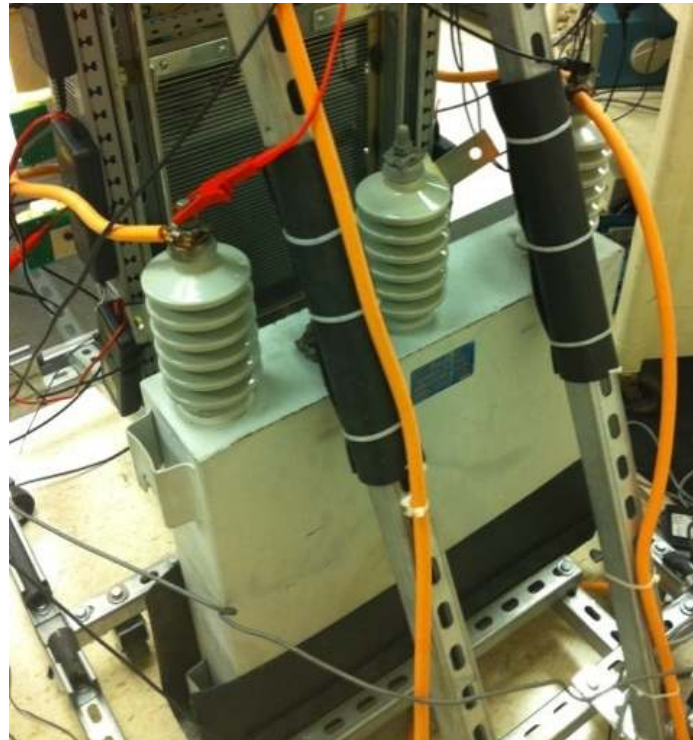
The VAR compensation capacitor used in the medium voltage prototype is a 300 kVAr 4.16 kV Westinghouse three-phase wye connected capacitor with a grounded neutral. Initial tests have been performed to determine component parasitics.

The component parasitics are determined by performing a self resonant frequency test using sine waves of different frequencies. At low frequencies the capacitor exhibits capacitive characteristics, i.e. as the frequency is increased the reactance of the capacitor decreases. At frequencies above the resonant frequency, the inductance (ESL) of the capacitor dominates and the reactance of the component increases with increasing frequency. At the resonant frequency the capacitive and inductive reactance's cancels out leaving the ESR (equivalent series resistance) of the capacitor as the dominant component.

It is important to understand the parasitics of the VAR compensation capacitor in order to minimize the impact of these parasitics on the operation of the ILSTATCOM. Determining the ESL of the capacitor is critical in estimating the loop inductance for the 3-level boost converter. The ESL will be used to calculate the capacitance required in the circuit to ensure low loop inductance. Parameters of the VAR compensation capacitor are given in Table 10.4



(a)



(b)

Figure 10.2: (a) ESL of capacitor for 3-level boost converter, (b) shunt compensation capacitor used for laboratory prototype.

Table 10.4: Parameters of VAR compensation capacitor

Parameter	Symbol	Value
Capacitance	C	23.5uF
Equivalent series inductance	ESL	100nH

10.3.2 BOOST INDUCTOR

The ratings used to design the boost inductor are shown in Table 10.3. The inductor is calculated for a specific value of current ripple and switching frequency. The inductor is designed for boost operation, i.e., 20% short term overvoltage on the output capacitor. At this operating point, the peak to peak current ripple of the inductor current is assumed to be 40%.

Table 10.5: Ratings for normal and boost operation

Normal operation (C = 47 uF)	Boost operation (C = 47 uF)
V = 2400V	V _{BOOST} = 2880V
I _{CRMS} = 2400/X _C = 2400/56.44 = 42.5A	I _{CRMS_BOOST} = 2880/X _C = 2880/56.44 = 51.09A
I _{pk} = 60.14 A	I _{Cpk_boost} = 72.17 A
I _{L_pk} = 60.14 A	I _{L_pk_boost} = 86.6 A

The equation for the boost inductor is shown below. For the values given in Table 10.5, the inductance is calculated to be 1.2 mH.

$$L = \frac{D(1-D)^2}{f \cdot \delta} \left(\frac{V_S^2}{Q} \right) = 1.2mH \quad (10.1)$$

Here, f is the switching frequency, δ is the % peak to peak current ripple, V_c is the voltage across the VAR compensation capacitor, and Q is the output reactive power.

From Equation 10.1, it can be seen that the inductance is dependant on the switching frequency, duty cycle, current ripple, output voltage, and output power.

Design of the inductor for the given operating condition is challenging as the core material of the inductor needs to have bidirectional excitation with a low AC operating flux and permeability for the given value of inductance. The core material selected is a powder core from Micrometals. To prevent saturation at higher currents, a stacked core design is used. It is assumed that the line inductance contributes to the effective inductance connected to the converter, i.e. the total boost inductance. The line inductance is assumed to be 200 μ H. The 990 μ H is realized by series connecting 3 inductors design for 330 μ H each.

Properties of the core are included in Appendix B. Basic design parameters obtained for the specific core material are shown below. An optimum design with a conservative design margin is developed by stacking three cores.

Table 10.3: Single core design values

SINGLE CORE	
A_L	$= 58 \text{ nH/N}^2$
A	$= 18.4 \text{ cm}^2$
L_m	$= 39.9 \text{ cm}$

The following values are design parameters obtained by stacking three cores. Using the three stacked core design parameters, the flux density and number of turns are calculated as:

Number of turns (N) = 51 turns (#8 awg, 3 strands)

$$B = \frac{L \cdot I_{L_pk_boost}}{N \cdot A} = \frac{330 \cdot 10^{-6} \cdot 86}{51 \cdot 36.8 \cdot 10^{-4}} = 0.151 \text{ T} \quad (10.2)$$

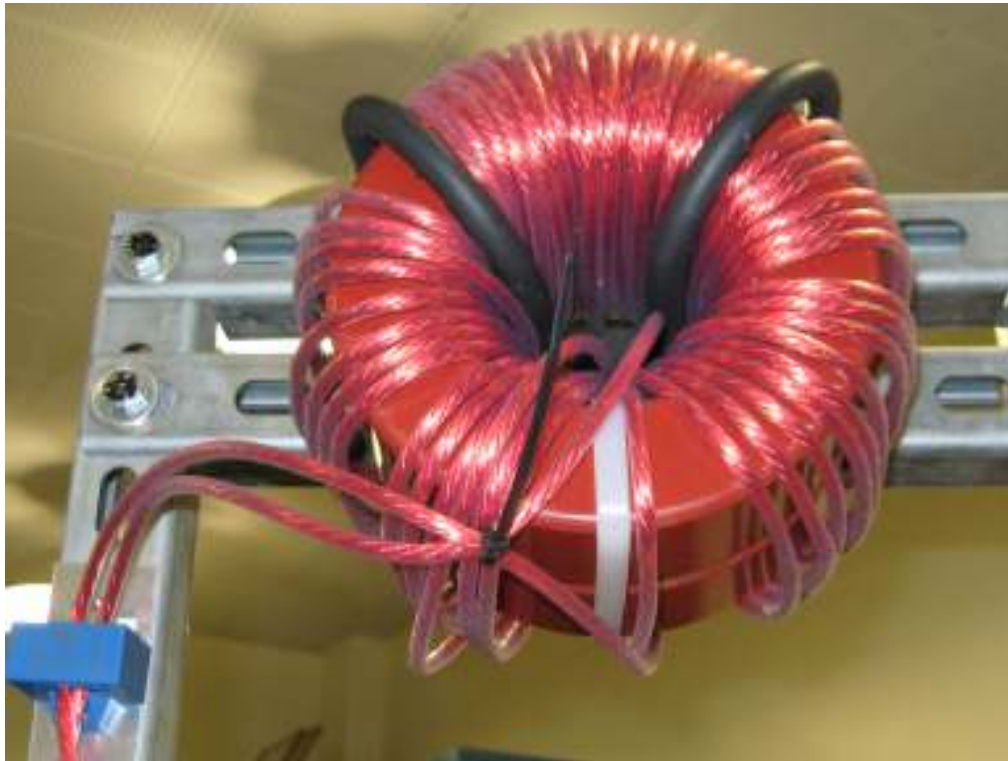
Here, B_{pk} for -2 material is 0.5T, L is the inductance, $I_{L_pk_boost}$ is the peak current through the inductor, N is the number of turns, and A is the cross-sectional area of the core.

Table 10.5: Results obtained using Micrometals design software

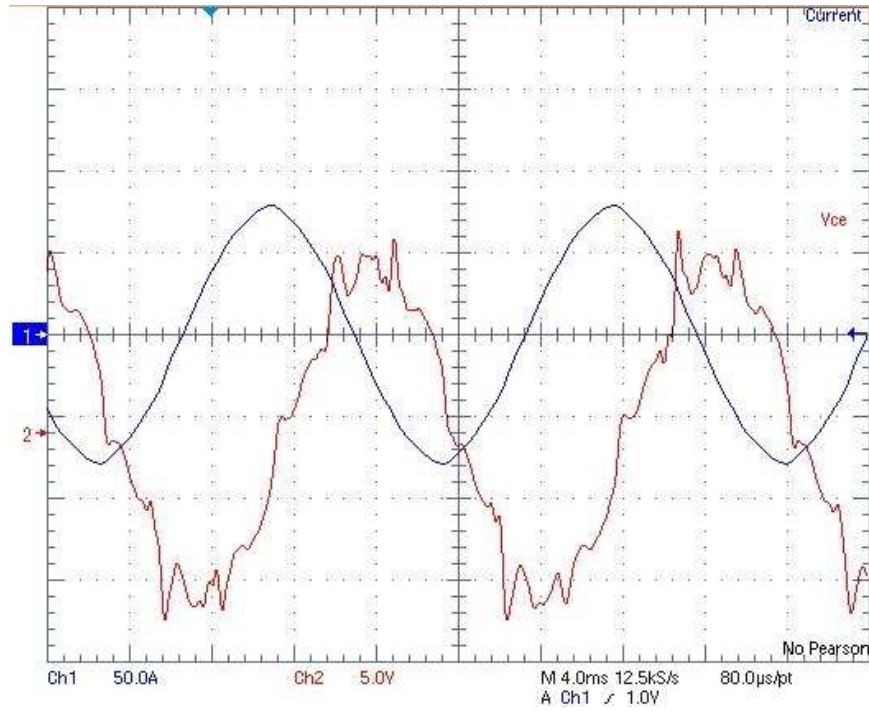
PRINT	ELECTRICAL	MECHANICAL	DC PERM	AC PERM	INDUCTANCE	LOSS	T RISE
POWERLINE FREQUENCY INDUCTOR ANALYSIS						Wed Apr 01 14:03:36 2009	
CORE PART NUMBER	1650-2	X	2	NUMBER IN STACK			
WIRE GAGE	# 8 AWG	X	3	STRANDS			
NUMBER OF TURNS	51.00						
AC CURRENT	50.00	AMPERES RMS					
FREQUENCY	3000.00	HERTZ					
AMBIENT TEMPERATURE	55.0	DEGREES C					
						<input type="button" value="OK"/>	
INDUCTANCE	314 u	Henry	CORE LOSS	86.7	W		
DC RESISTANCE	11.9 m	OHMS	COPPER LOSS	29.7	W		
AC RESISTANCE		OHMS	BUILD	0.233	in		
RIPPLE CURRENT		AMPS p-p	SURFACE AREA	1047.4	Sq cm		
DC BIAS		OES	TEMP RISE @ 0 HRS	50.6	DEG C		
AC FLUX DENSITY	1185	GAUSS	TIME TO 115 % LOSS	1.07e+05	HOURS		
PERCENT PERM	104	PCT	LIFE LIMIT	6.6e+05	HOURS		
CORE AL VALUE	116	nH					

As the final prototype will be tested at a current lower than the actual design value, the final design validation has been done for a two core design. The design has been verified using the design software available from Micrometals. The final results (for a 2 core design) are shown in Table 10.5.

Figure 10.3(a) illustrates the inductor. For the current rating of 50Arms, 8AWG litz wire is used. The inductor has been tested at a current of 54A. The inductance has been measured to be 370 μ H with no saturation. Voltage across the inductor and current through the inductor I_L is shown in Figure 10.3(b).



(a)



(b)

Figure 10.3: (a) Inductor, (b) Voltage across L at $I_L = 54A$.

Each inductor requires 51 turns of an 8AWG wire. This is challenging because of the relatively small inner diameter of the cores and the stiffness of the wire. Litz wire is therefore used. In addition to the insulated strands, the wire is custom designed with a PVC jacket to provide increased the turn-to-turn insulation strength.

10.3.3 FILTER CAPACITOR

Selection of the filter capacitor is based on the operating voltage, modulation technique, and percent voltage ripple. For the 3-level converter the voltage impressed across the filter capacitor C_f is 0.5 times the voltage across the VAR compensation capacitor. Under normal operation rms voltage across the filter capacitor is 1.2kV, while under boost operation the voltage across C_f is 1.44kV.

The modulation technique used to control the voltage across C_f , as discussed in Section 6.4.1.3, requires the capacitance to be a fraction of the capacitance of the VAR compensation capacitor. For the given experimental prototype the following factors have been used to select the component:

1. Component lead times
2. $C_f \approx C/5$

The ratio of C to C_f has been selected to maintain granularity of control while ensuring C_f smaller than C so that the overall time needed to charge the capacitor C_f to the desired voltage is relatively small.



Figure 10.4: Filter capacitor.

The capacitance has been chosen to be $11.67\mu\text{F}$. This is equal to 25% of the capacitance of the VAR compensation capacitor. The $11.67\mu\text{F}$ at a maximum of 1440V is achieved by series connecting 3 capacitors rated at 900V with a capacitance of $35\mu\text{F}$, as shown in Figure 10.4.

10.3.4 SNUBBER COMPONENTS

The issues with sequencing and commutation that are inherent to AC converters are a critical part of the implementation and hence need to be addressed in detail. The AC switch configuration used is a common-emitter IGBT based switch as shown in Figure 10.5. Commutating current between AC

switches is non-trivial as the current needs to be transferred from one AC switch to another while ensuring that the current always has a path to flow and the driving voltage source in the loop is not short circuited. Commutation in AC-AC converters is usually implemented in four steps. Each of the four steps involves sequentially turning ON or OFF an IGBT based on the polarity of the current, or voltage, or both. Details of the commutation method are included in Section 6.4.2. Device commutation in the experimental prototype has been implemented using multiple commutation methods. The first is a simple four-step commutation technique based on current direction. This technique has been extensively researched and documented. Through the testing process various commutation techniques have been tested to understand the implications of each method. Details will be presented in the latter part of this chapter. Complexities in implementation of all the tested methods arise primarily from the lack of accurate current and, or voltage measurements. Regardless of the commutation method it is essential to have a safety-net in case of inaccurate measurements and faults in the converter. Snubbers are used in the converter as a safety-net. The snubbers used in the ILSTATCOM are passive and provide a path for the current to flow in case of missteps in commutation. The snubbers also provide a path for the dissipation of energy in the event of a fault.

The snubber used in this AC-AC converter is an RCD snubber i.e., each snubber comprises of a diode, resistor and capacitor. Different passive snubbers have been considered for the ILSTATCOM prototype, as shown in Figure 10.5.

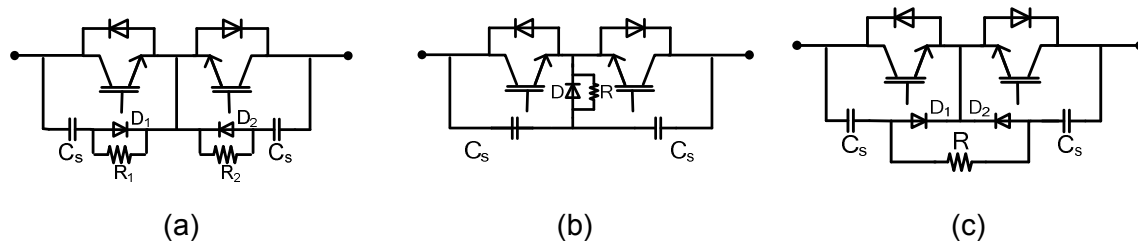


Figure 10.5: Snubber circuits

Figure 10.6 shows the 3-level ILSTATCOM boost converter with the final snubber selection. Operation of the snubber is fairly simple, where each capacitor charges to the peak of the driving voltage of the cell. As an example, the snubber of device S6 charges to the peak of $V_c - V_{cf}$.

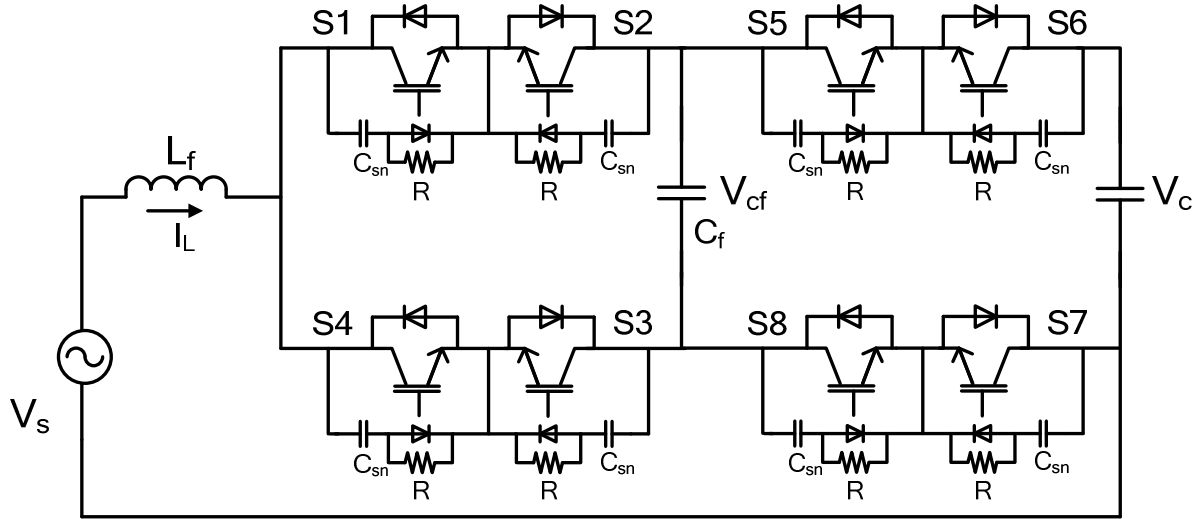


Figure 10.6: 3-level AC converter with snubber implementation

Operation of the snubber requires characterizing the RC time constant with respect to the fundamental frequency of the input voltage. To ensure minimal losses in the snubber the RC time constant is chosen to be ten times the fundamental frequency, i.e.,

$$\tau = R \cdot C \cong 160\text{ms}$$

The voltage and current ratings of the snubber components are listed in Table 10.6.

Table 10.6: Rating of snubber components.

Snubber Component	Rating
Capacitor	$\sqrt{2}V_s$
Resistor 'R'	$R = \frac{\tau}{C}$ $P_R = \frac{1}{2}C \cdot \Delta V^2 f_{sw}$

Where ΔV = the drop in the capacitor voltage.

f_{sw} = switching frequency

Selection of the snubber has been made based on detailed computer simulations.

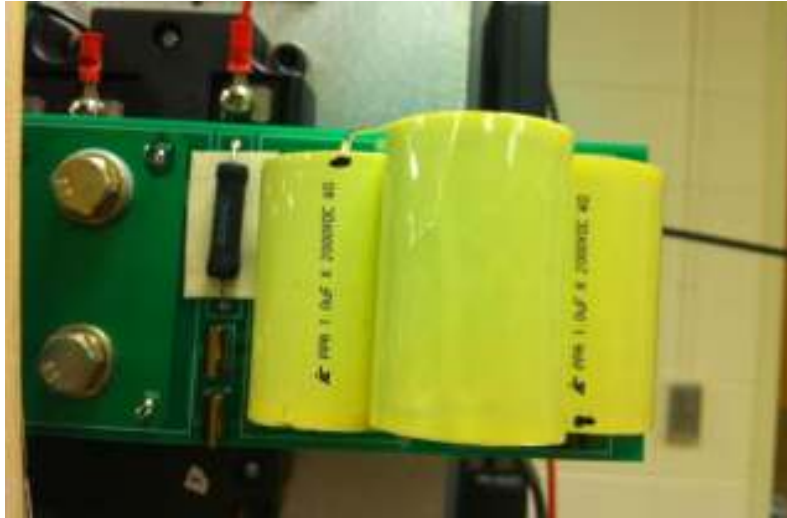


Figure 10.7: Snubber circuits

The simulation results for the snubber configuration selected for the 3-level ILSTATCOM is shown in Figure 2.5. Results for the different snubber parameters are illustrated in this section. The two cases considered are for $\tau = 175\text{ms}$ and $\tau = 875\text{ms}$.

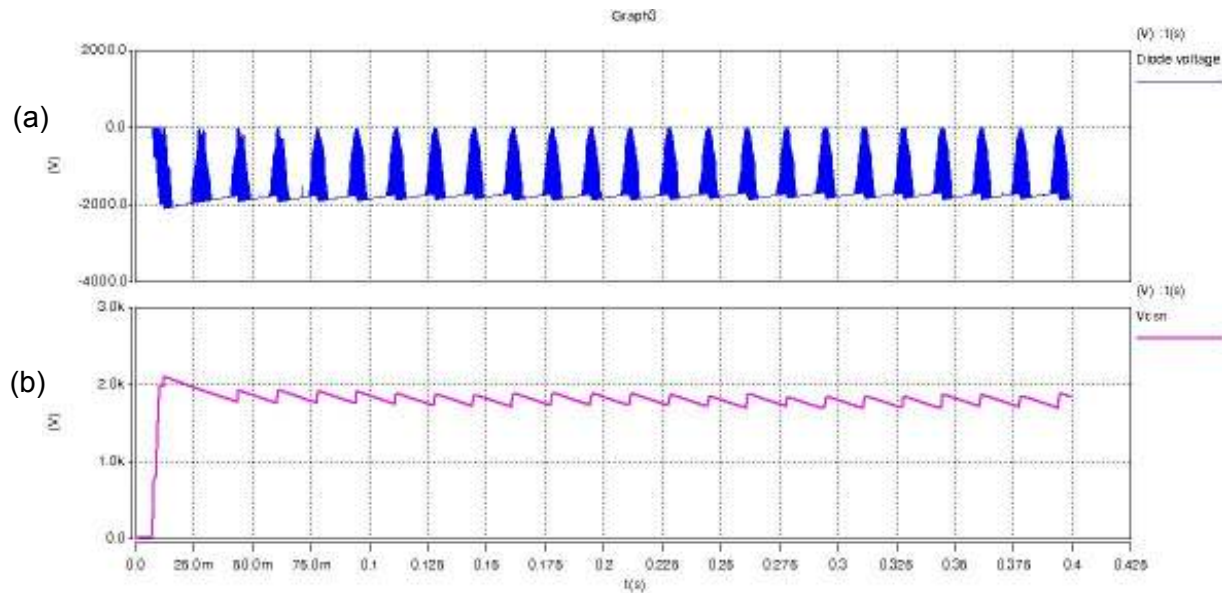


Figure 10.8: 3-level AC converter with snubber implementation $\tau = 175\text{ms}$, (a) diode voltage, (b) voltage across snubber capacitor

The simulation results show operation of the snubber. The voltage across the capacitor is roughly at 0.5 times the supply voltage, this is because the filter capacitor is regulated to 0.5 times the output capacitor voltage. Rate of discharge of the capacitor voltage is dependant on the selection of the time constant, in this case RC time constant is chosen to be about ten times the supply frequency.

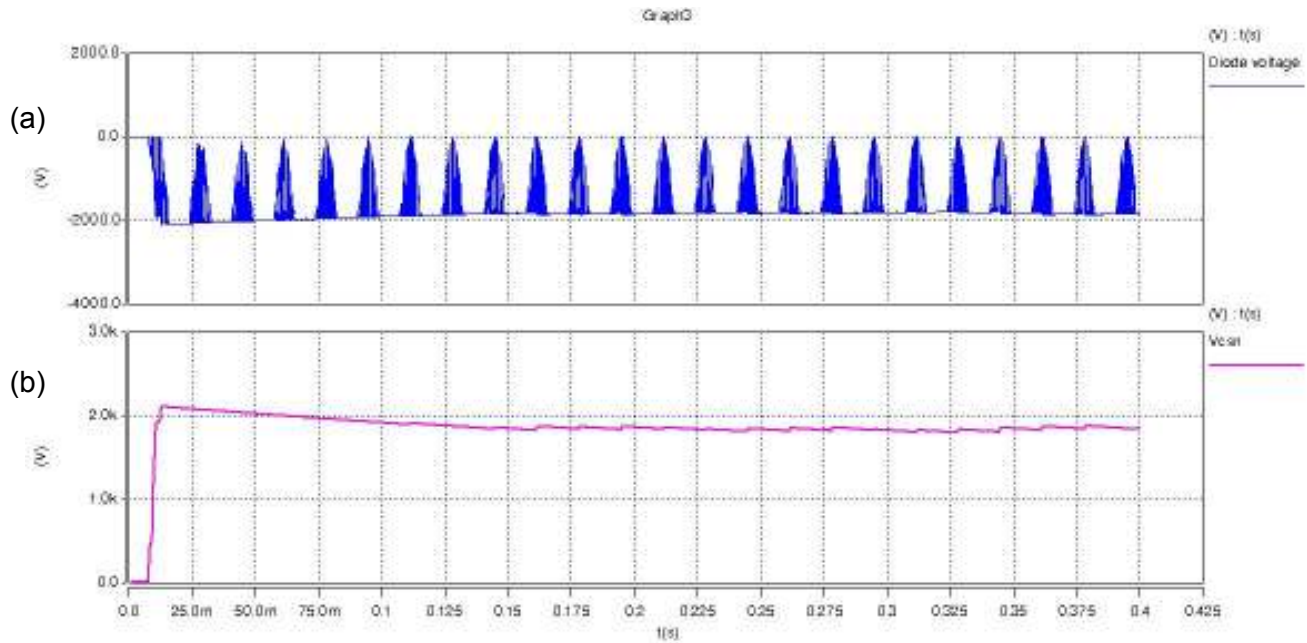


Figure 10.9: 3-level AC Converter with snubber implementation, $\tau = 875\text{ms}$, (a) diode voltage, (b) voltage across snubber capacitor

Based on the results of initial tests the snubber capacitor has been increased to $2.5\mu\text{F}$. The time constant of the snubber for the final results is 875ms .

10.3.4 BUS PLANE COMPONENTS

Bus planes are used to make electrical connections between the various components in the ILSTATCOM. The bus plane is formed using alternate layer of copper sheet, Nomex insulation, and Kapton sheets. The thickness of the copper sheet is selected based on the required current capacity. In this case, for ease of fabrication the thickness of the copper sheets is selected to be greater than what is required. Copper sheets are stacked with layers of Nomex and

Kapton between two adjacent layers of copper sheets. Both Nomex and Kapton are used because of the different properties of each material. The thickness and dielectric strength of the sheets are given in Table 10.2. Figure 10.10 illustrates the bus planes.



Figure 10.10: Bus planes

10.3.5 IGBT SELECTION AND CHARACTERIZATION

The IGBTs selected for the medium voltage 3-level ILSTATCOM is 3.3 kV Dynex single IGBT. Two IGBTs are connected in a common-emitter configuration to realize a single AC switch. As part of the implementation, each IGBT is characterized to understand device parameters. A device characterization setup with standard two pulse control is implemented. Details of the results are included in Appendix C.

A typical waveform obtained using the device characterization setup is shown in Figure 10.11. V_{ce} , I_c , P_{cond} and P_{sw} are obtained for each device using this waveform.

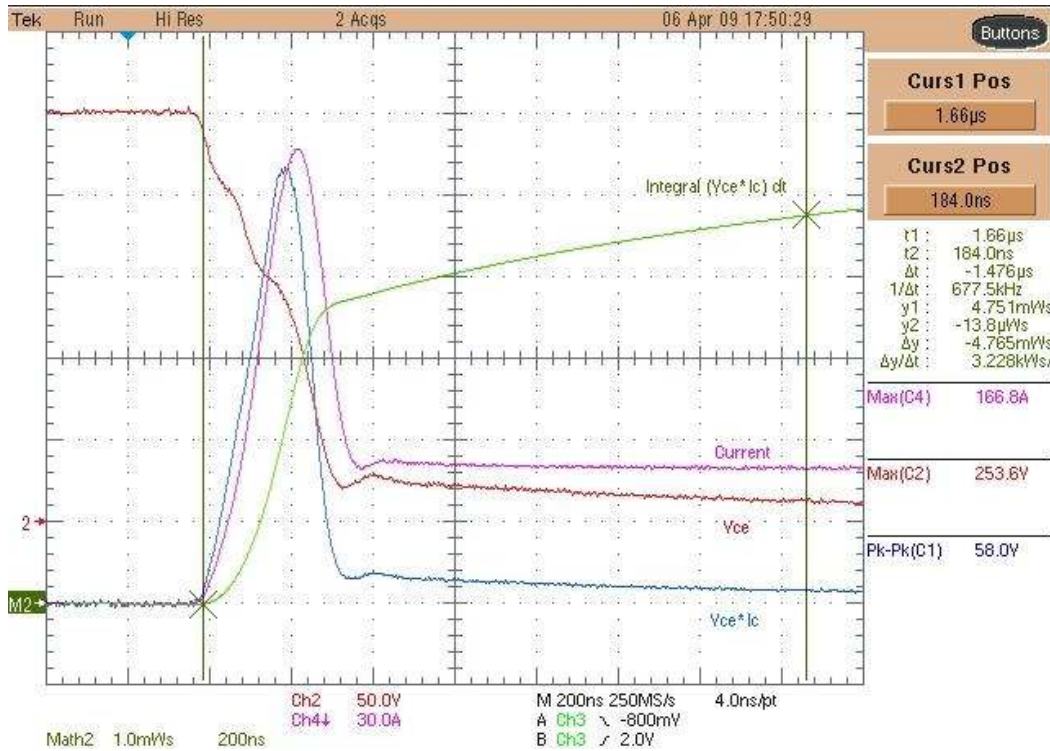


Figure 10.11: V_{ce} , I_c , P_{cond} , P_{sw}

10.3.6 SENSORS

Voltage and current measurements are required for converter control. Three sensors are used, two voltage and one current sensor. The voltage sensors are used to measure the voltages across the filter capacitor and VAR compensation capacitor. Current sensor is used to measure the inductor current. Details are included in Table 10.3.

10.3.7 MECHANICAL DESIGN

Mechanical layout of the converter has been developed based on the components selected. The final layout is illustrated in Figure 10.12. Illustrations of the prototype are shown in a later section.

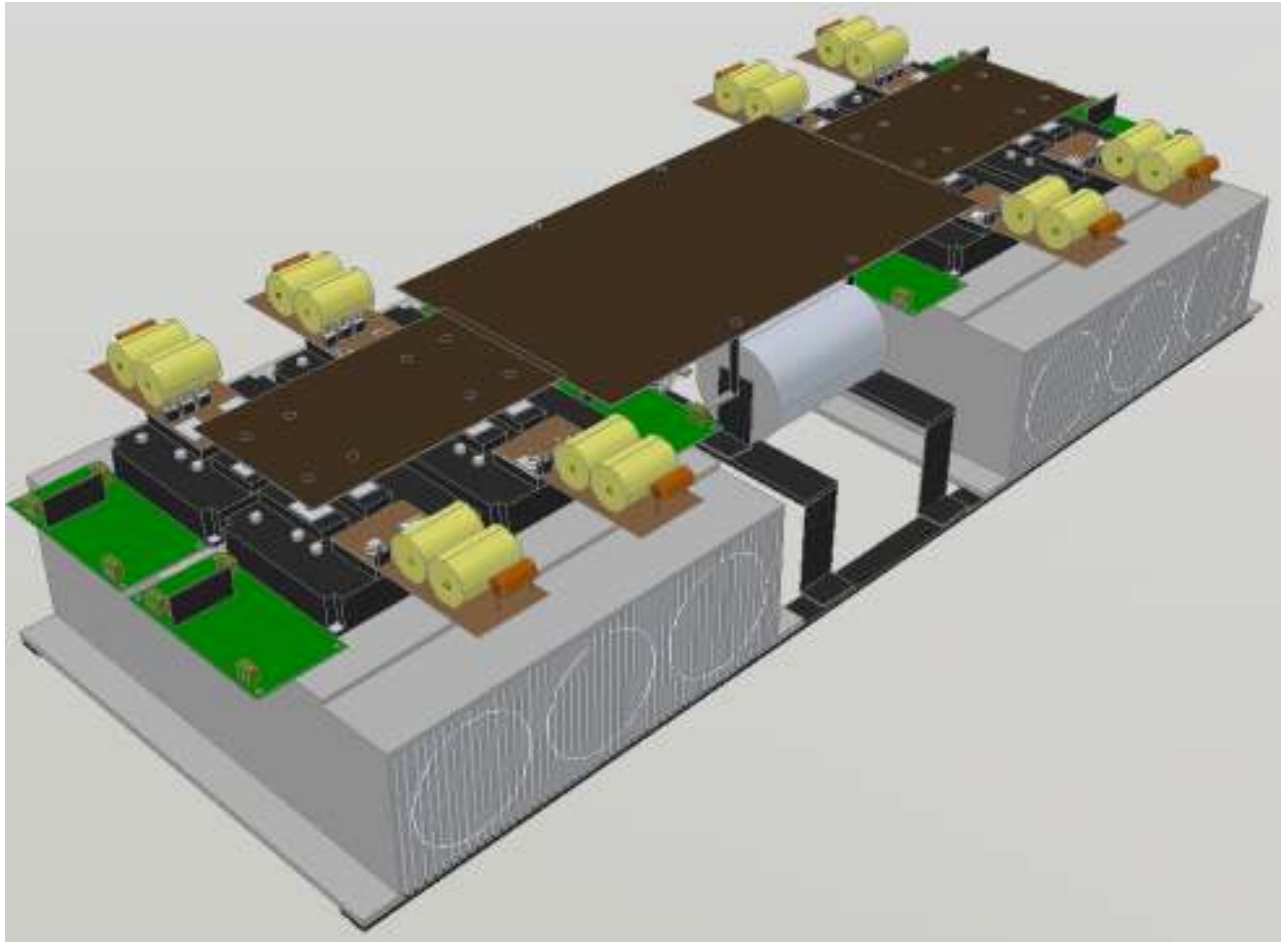


Figure 10.12: Mechanical layout of converter

The converter has been designed to be vertical. A frame has been built, on which the converter has been mounted, shown in Figure 10.13 and 10.14.





Figure 10.13: Mechanical layout of converter

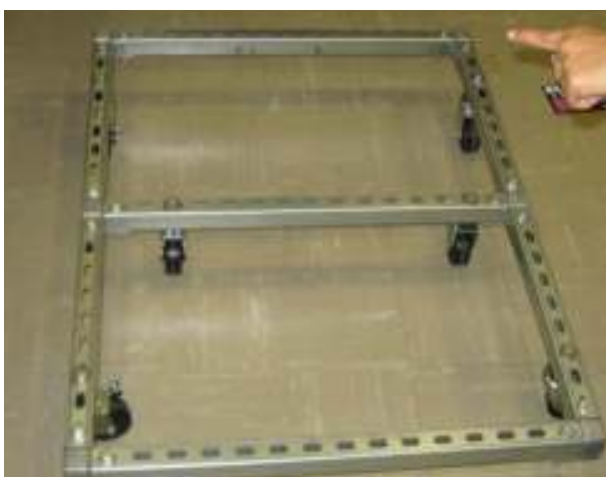


Figure 10.14: Converter frame

10.3.8 DEVICE LAYOUT

Thermal analysis of the converter has not been done for the prototype. The physical size of each IGBT has dictated the dimensions of the heat sink. Given the operating power level and size of the heatsink, the converter is thermally over-designed. Layout of the devices is illustrated in Figure 10.15.

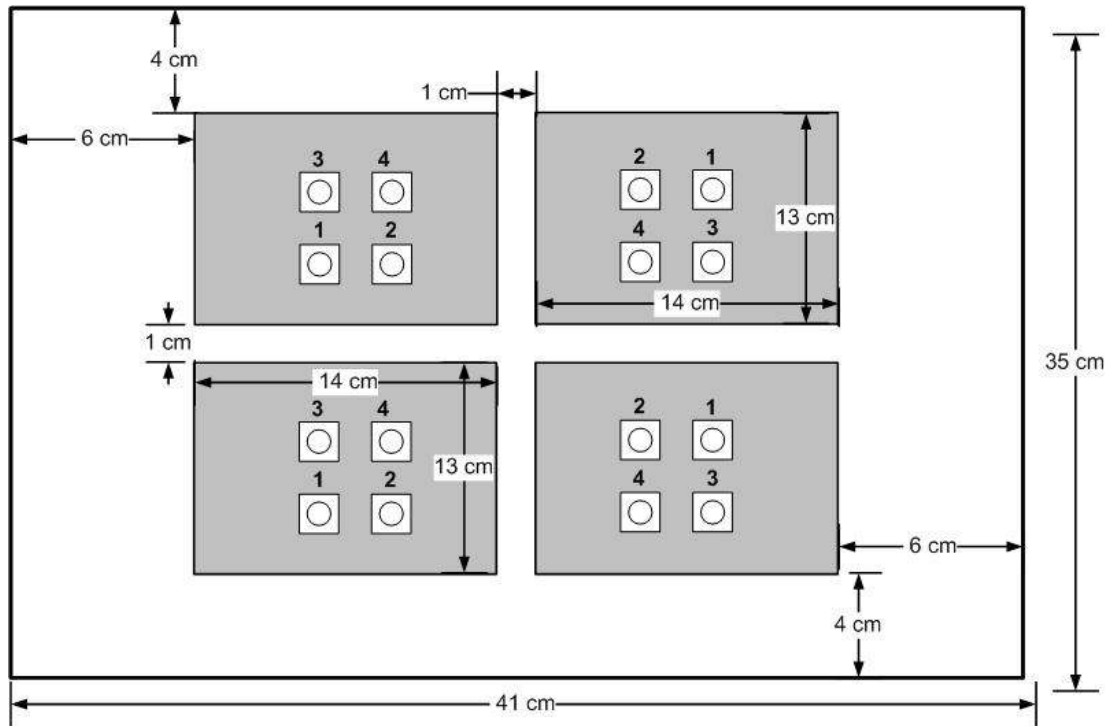


Figure 10.15: Device layout on heatsink

10.4 CONTROL PLATFORM

The control platform used in the ILSTATCOM prototype is illustrated in Figure 10.16. The control board interfaces with the IGBT gate drives and voltage and current sensors. Signals interfacing with the control board are both fiber optic signals and analog signals. Fiber optic signals are transmitted and received from the control board. Gate pulses are transmitted to the gate driver boards for each device and fault signals from the gate drive boards are received at the control board and further processed through a logic circuit, and finally sent to the DSP as a single FAULT signal for each cell, shown in Figure 10.16.

Analog signals received from the voltage and current sensors are level-shifted and scaled by appropriate gains to give 0 to 3.3V signals that are used by the DSP to determine quadrant information. Gate pulses are generated by the DSP based on the duty cycle for each cell and quadrant information obtained using voltage and current measurements. The output of the DSP is quadrant information and the duty cycle for each cell. These signals are then used by the state machine to generate the gate pulses for each of the eight IGBTs.

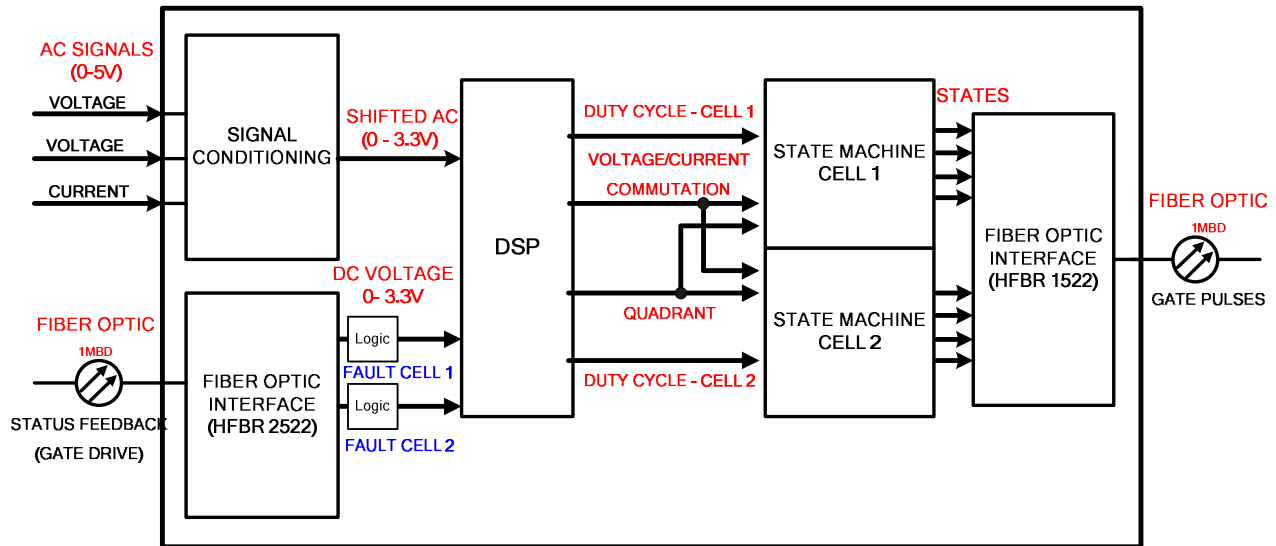


Figure 10.16: Schematic of control platform

The gate pulses are transmitted to the gate drive boards that drive the devices. An eight layer control board has been designed using Eagle. The final board is shown in Figure 10.17. The control board and gate drives are fed from a single DC power supply rated at 110W.



Figure 10.17: Control board and power supply

10.5 STATE MACHINE

State machine for the 3-level ILSTATCOM is the most complex part of the design process. The initial approach was to operate the converter with a current direction-based commutation scheme. Current direction-based commutation offers safe commutation between AC switches, provided snubbers are used. The advantage of using this mode of commutation is in the ability to prevent shoot through's in each cell, i.e., short circuiting of the driving voltage source in each cell. The worst-case scenario using this commutation mode is when both switches (that are required to be ON) are in an OFF state. This results in the current having no path to flow. This causes voltage spikes that could potentially destroy the devices. The state machine developed using current commutation is shown in Figure 10.18. There are eight legal states in this mode, two final states and six intermediate states. The intermediate states are used to transition between the final states using a four-step commutation process (assuming current commutation, as explained in Chapter 7). To ensure minimal impact of the four-step commutation process on the output parameters the state machine needs to operate at a frequency significantly higher than the switching frequency. For this prototype a switching frequency of 3 kHz is used for the converter and the state machine is operated at 500 kHz (clock frequency).

The state machine in the ILSTATCOM prototype is implemented using an EEPROM and Latch. Figure 10.18 illustrates the structure of the state machine. Each cell is operated with its own state machine. For this converter the state machines do not have any common inputs, i.e., all quadrant information etc. is determined separately for each cell. The state machines are however clocked simultaneously to ensure synchronized commutation between cells, thereby enabling control and commutation of the multilevel converter as a whole. Each state machine has eight inputs, four of which are fed back from the latch.

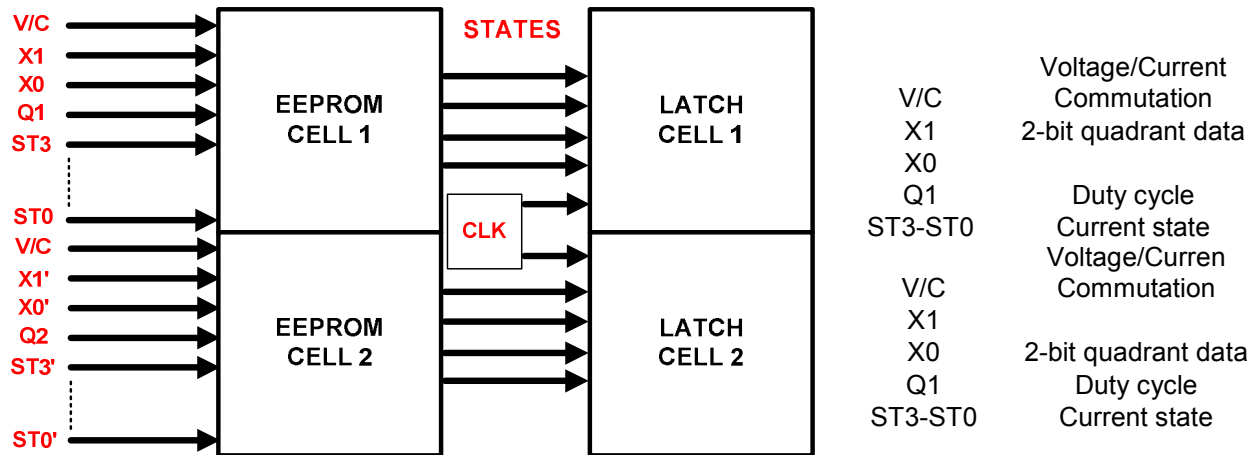
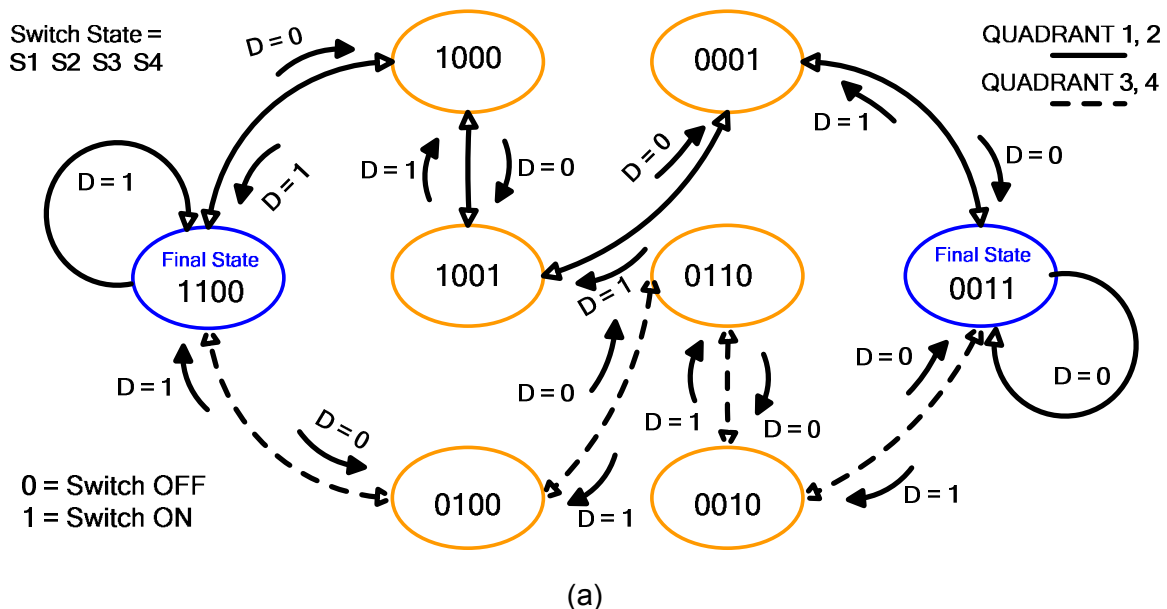


Figure 10.18: Control board and power supply, (a) schematic, (b) list of variables

10.5.1 CURRENT COMMUTATION

Current commutation is discussed in detail in Chapter 7. For completeness the state machine used for commutation is shown in Figure 10.19. Current commutation is used to transition from State 12 to State 3 and back. Transitioning between final states requires knowledge of the current direction and the present state of the converter cell. Uncertainty in any one of the parameters will result in an incorrect commutation step and possibly a voltage spike. To alleviate problems with incorrect commutation sequences snubbers are used.



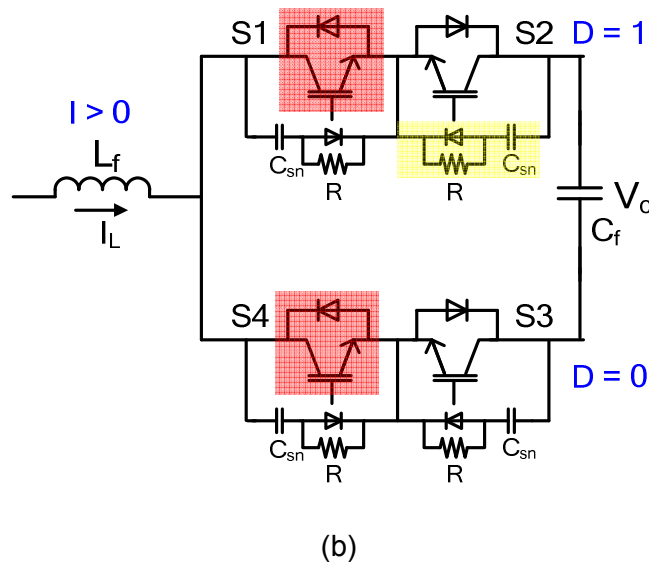


Figure 10.19: State diagram for current commutation

As an example, consider the cell shown in Figure 10.19(b). Commutating from S1, S2 to S3, S4 for positive current ($I > 0$) will require transitioning through state 1010. If at time $t = t_1$, the current changes polarity, there is no path for the current to flow. The snubber for S2 will thereby provide a path for the current until the state machine corrects for the change in current polarity.

Following the implementation method described in Figure 10.18, it is important to note that constructing the state machine is a detailed and tedious process. Even though there are only eight legal states, there are in actual fact a total of 256 memory locations that represent a combination of voltage and, or current commutation mode, quadrant, present, state, and duty cycle. All combinations need to be treated as a possible state transition in order to develop a fool-proof state machine that allows transitions to a safe state regardless of whether the converter is a legal or illegal state.

10.5.2 VOLTAGE COMMUTATION

Voltage commutation is commutation based on the polarity of the driving voltage. The basic principle involves determining the devices that are forward biased based on the polarity of the cell driving voltage and commutating between

the reverse biased devices. This mode of commutation can be performed in two and four-steps, as shown in Figure 10.20 and 10.21 respectively.

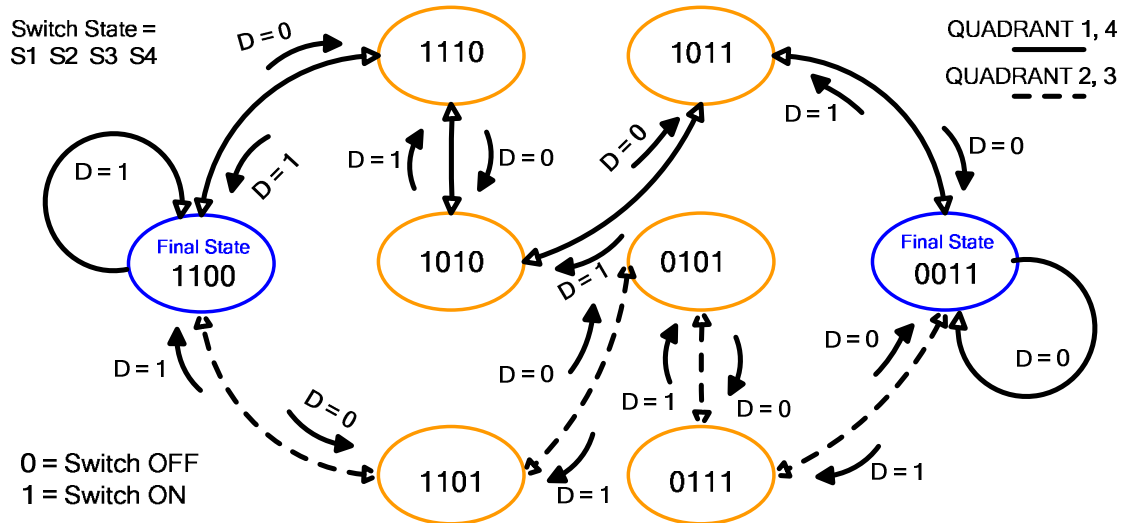
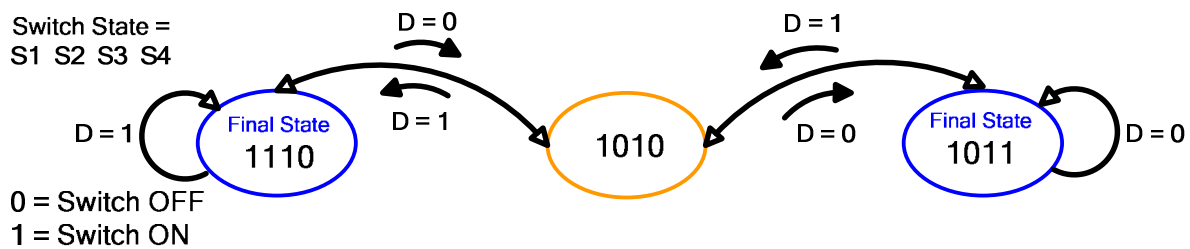


Figure 10.20: State diagram for 4 step voltage commutation

While voltage commutation is a much simpler method compared to current commutation it can be catastrophic if there is a misstep in commutation. Errors during commutation that occur during current commutation can be taken care of by the use of snubbers. The same cannot be done for voltage commutation. Any misstep in commutation will result in the short circuit of the cell. Figure 10.22 illustrates the impact of missteps in voltage commutation. It is therefore extremely important to have a very accurate reading of the cell driving voltage. This becomes quite challenging when the voltage waveform is close to the zero-crossing.



(a)

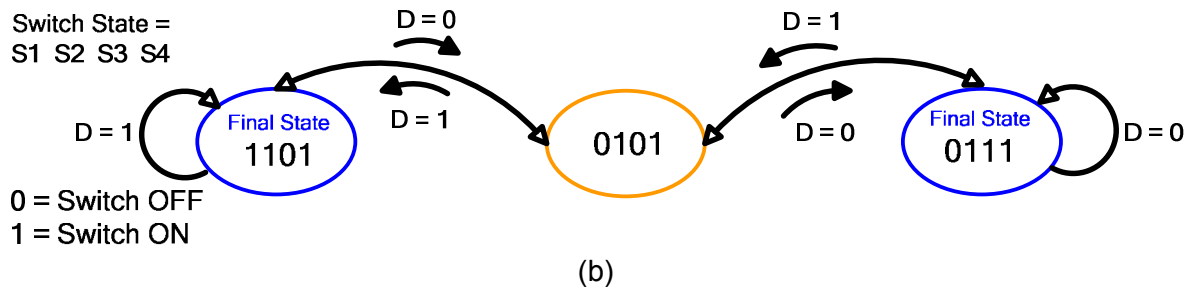


Figure 10.21: State diagram for 2 step voltage commutation, (a) $V > 0$, (b) $V < 0$

Two-step voltage commutation is realized by ensuring the devices with forward biased diodes remain on for the corresponding half-cycles of the cell driving voltage. Switching between the reverse biased devices is then based on the duty cycle. This commutation method is similar to commutation in inverters. Four-step voltage commutation is possible by having final states that are the same as the final states in current based commutation. The intermediate states are then based on the polarity of the driving voltage. State diagrams are shown in Figures 10.20 and 10.21.

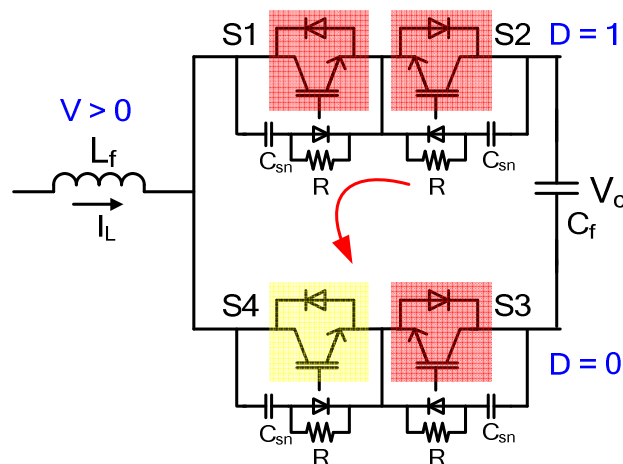


Figure 10.22: State diagram for two step voltage commutation, (a) $V > 0$, (b) $V < 0$, (c) illustration of misstep in commutation

The repercussions of a misstep in commutation during voltage commutation can be catastrophic, as mentioned earlier. To illustrate the same, consider Figure 10.22. For $V > 0$, and $D = 1$ (S1, S2 are ON) the cell is in state 1100. If the

voltage changes polarity, device S4 will be forward biased, resulting in a short circuit of the driving voltage V_c .

Based on the discussion so far on the various commutation methods, it is clear that any errors in signal measurements and missteps in commutation due to noise etc., could lead to failure of the converter.

10.5.3 VOLTAGE AND CURRENT COMMUTATION

The voltage and current commutation methods described so far are well researched and used widely in AC-AC converters. There are drawbacks of each method that have been illustrated to highlight the importance of commutation and the complexities and drawbacks of AC switch commutation. The commutation method developed in this section is used for the ILSTATCOM prototype. This commutation method is developed based on the 90 degree phase-shift between the voltage and current for a reactive power compensator, i.e., when the voltage is has a low value, the value of the current is high and vice versa, as shown in Figure 10.23.

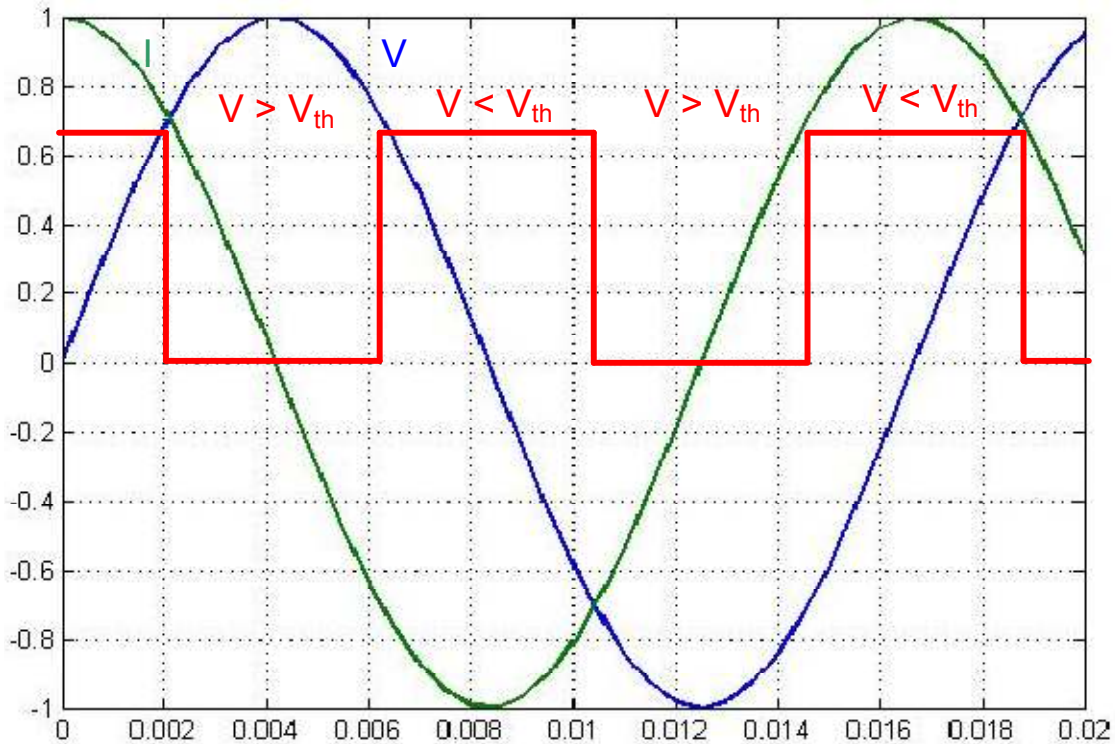


Figure 10.23: Hybrid commutation mode based on voltage and current

This characteristic allows the use of a hybrid commutation mode, where a selection can be made between current and voltage commutation based on the integrity of the measurement signals. The hybrid commutation mode is implemented by considering a threshold value for the voltage, where if $V > V_{th}$, voltage commutation is selected and if $V < V_{th}$, current commutation mode is selected. The assumption here is that if V is below V_{th} , the value of the current is significantly high thereby ensuring an accurate sensor measurement. Implementation of the method is such that every cycle of the fundamental frequency is divided into modes. Mode 1 is a current commutation mode and mode 2 is a voltage commutation mode. During each of the two modes commutation between AC switches is straightforward because it follows the methods described in the previous sections. The challenging part of this hybrid commutation method is the transition between voltage and current commutation modes. There are 2 methods that have been developed.

- Transitions based on current and voltage.
- Transitions based on
 - Voltage when going from current commutation mode to voltage commutation mode
 - Current, when going from current commutation mode to voltage commutation mode

The state diagrams for both methods are quite involved and have therefore not been included in full detail. An illustration of the thought-process is shown in Figure 10.24, where specific cases are considered. Multiple testing iterations have been carried out to determine the more robust method. The final experimental results illustrate hybrid commutation mode with transitions based on voltage and current information.

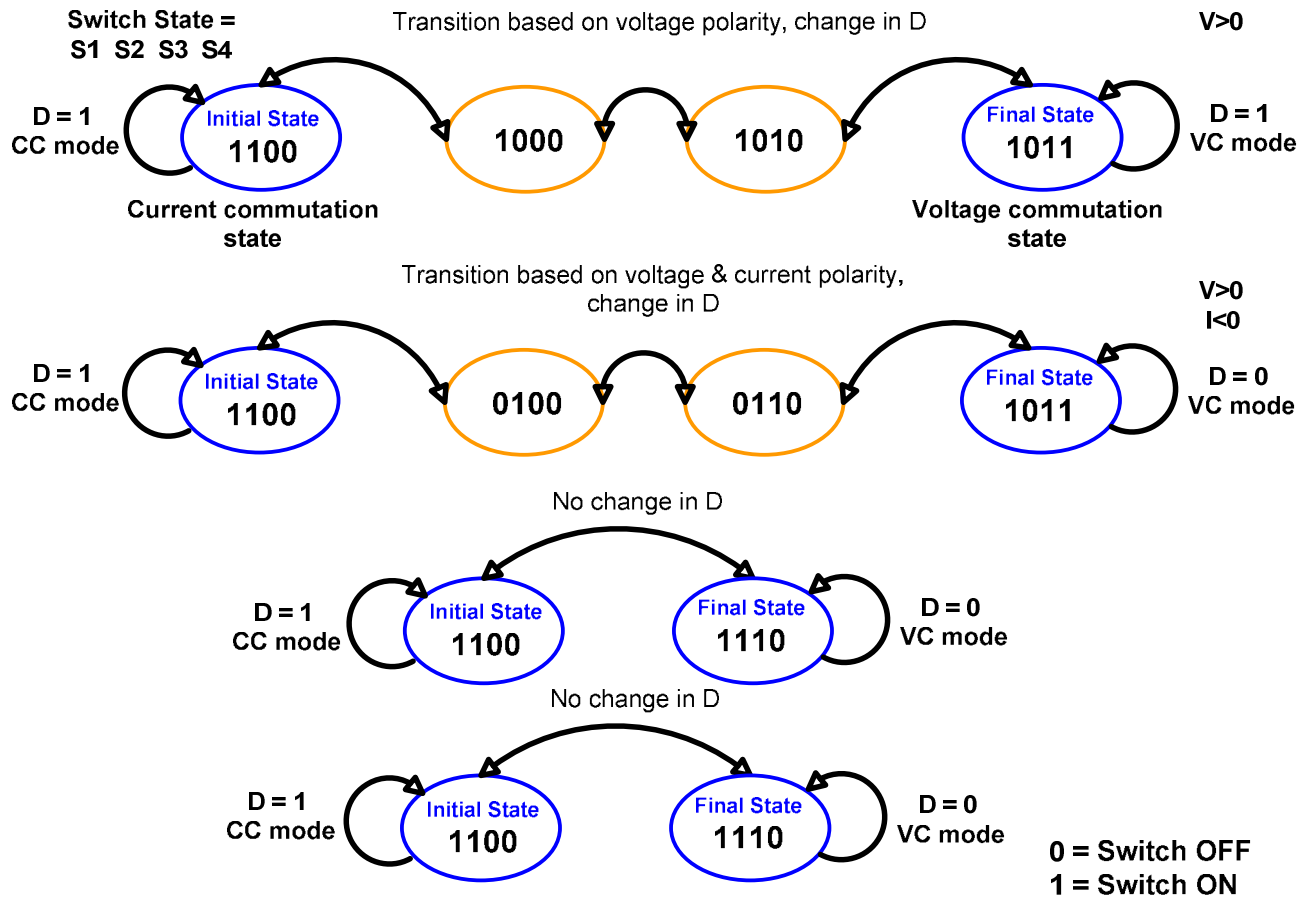


Figure 10.24: State machine for transitions from current commutation to voltage commutation mode and vice versa.

Through the testing of these algorithms certain changes have been made to the state machine. These changes have been made purely from an implementation stand point and are not required in theory. An example of this is shown in Figure 10.25, where, for no change in the duty cycle the current commutation state is taken through three steps to reach the voltage commutation state (which can be reached in a single state transition in theory).

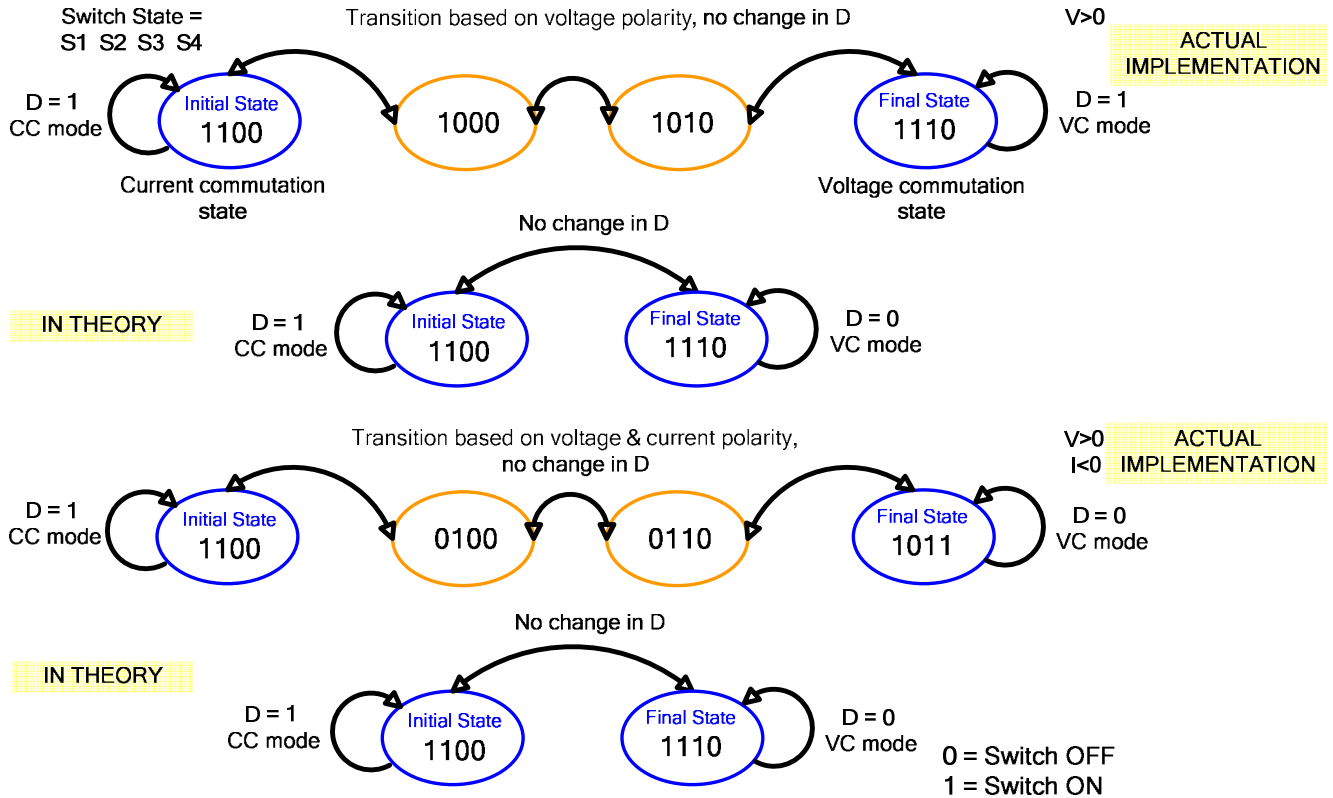


Figure 10.25: State machine changes for actual implementation.

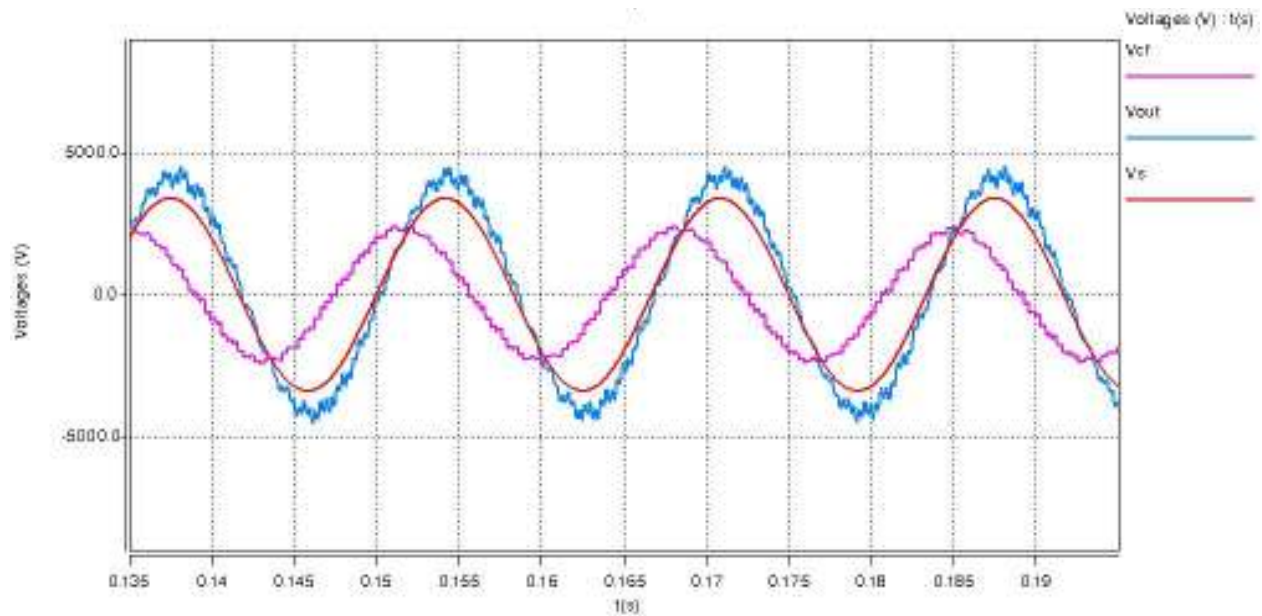
The primary reason for these changes is to avoid multiple uncertainties during a single instance, i.e., change in duty cycle and change in quadrant information. Experimental testing and verification of these algorithms is presented in the following sections.

10.6 SIMULATION AND EXPERIMENTAL RESULTS

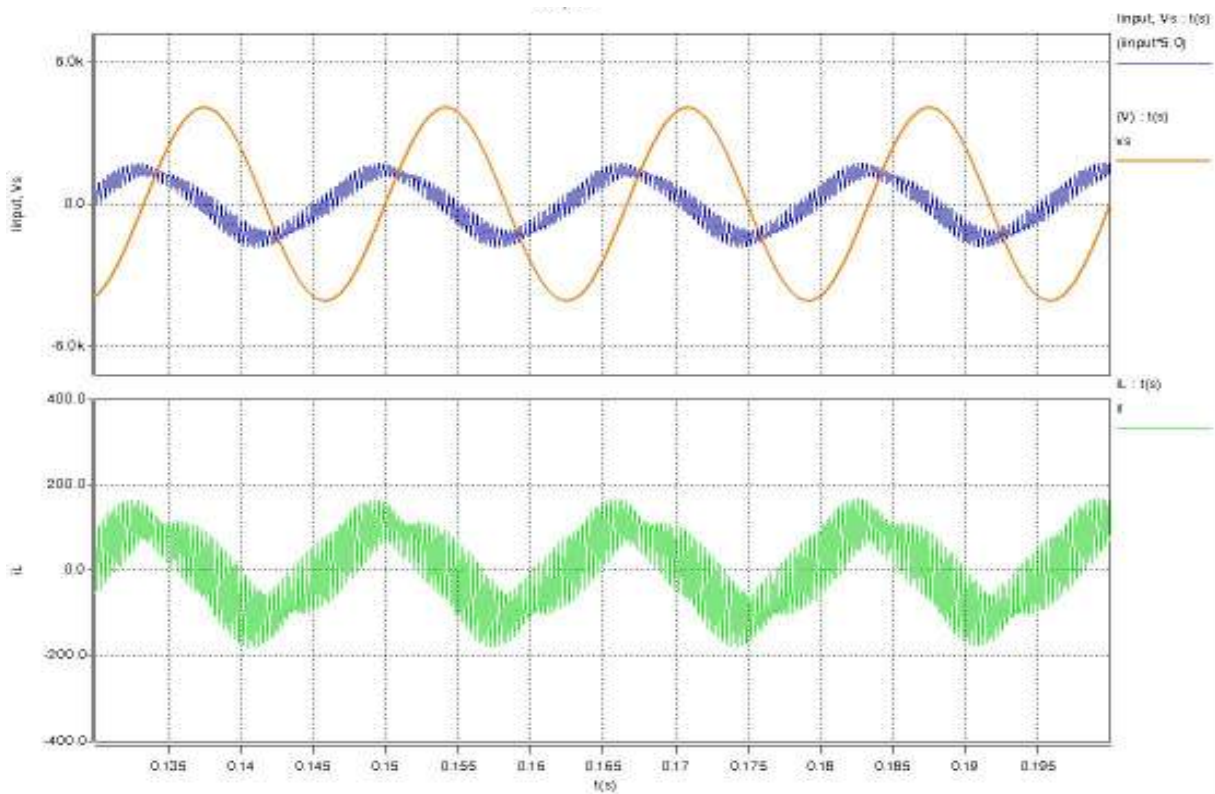
Simulation and experimental results for the final prototype are illustrated in the following section. A detailed simulation model in Saber has been built to validate the theoretical design. Complexities with the implementation of this design were dealt with and tested first using the simulation model and then experimentally.

10.6.1 SIMULATION RESULTS WITH INITIAL DESIGN

The following results illustrate the response of the system with the initial design values. Switch transitions in all the results are based on current commutation.



(a)



(b)

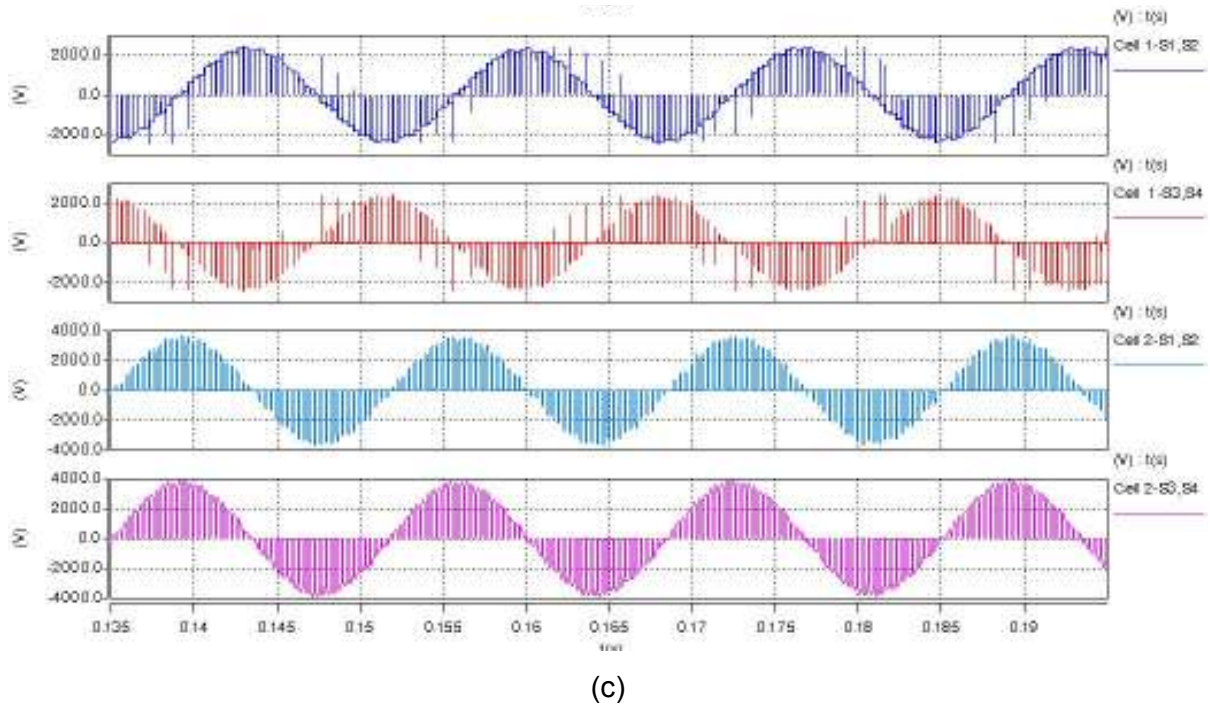
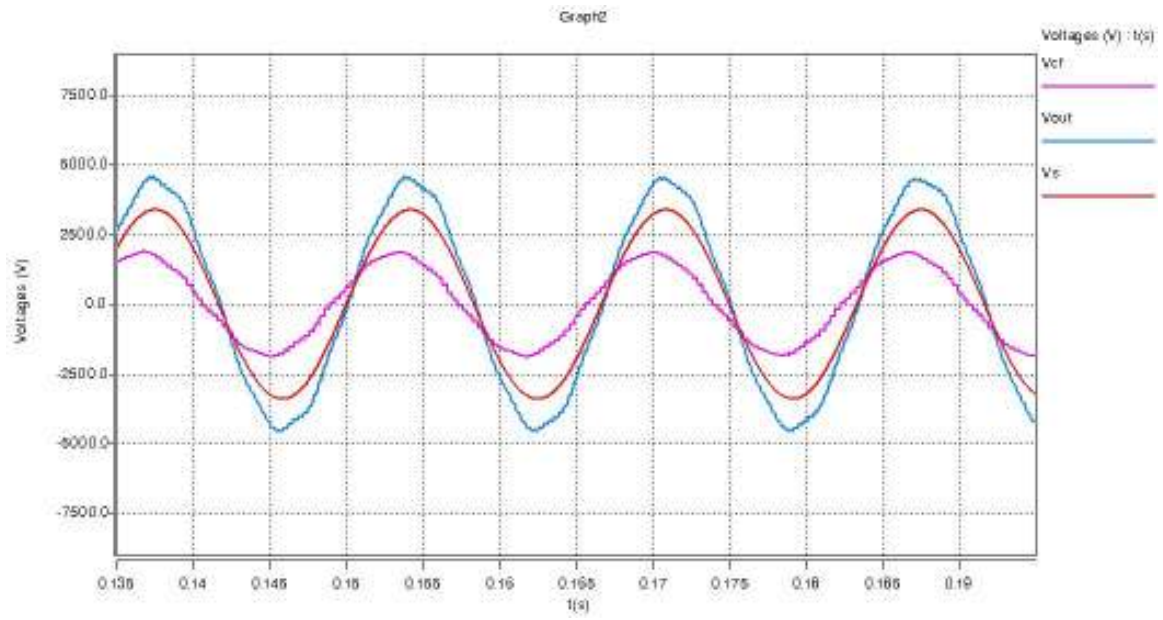


Figure 10.26: Simulation results for ILSTATCOM at 2400V and 20% boost, (a) V_s , V_{cf} , and V_c , (b) V_s , $5xI_{in}$, I_L , (c) AC switch voltages.

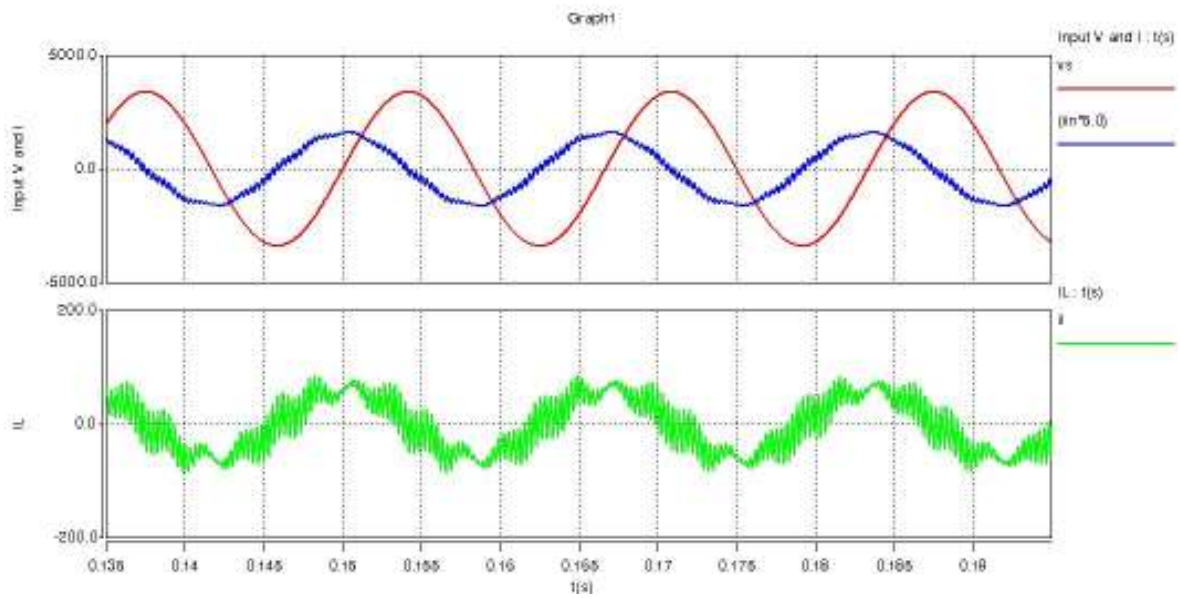
An important drawback of the initial design is the value of the boost inductor. The boost inductor was initially designed for a value of 1.2 mH, assuming a switching frequency of 7 kHz. Given the individual characteristics of the devices and gate drives, the converter switching frequency was reduced to 3 kHz. This results in a current that changes polarity almost every switching cycle. This was a serious problem because the current polarity measured and used in the state machine for the state transitions was different from the polarity during actual commutation. Efforts have been made to adjust the sampling instants to ensure the most recent current polarity with respect to the commutation sequence.

10.6.2 SIMULATION WITH MODIFIED BOOST INDUCTOR

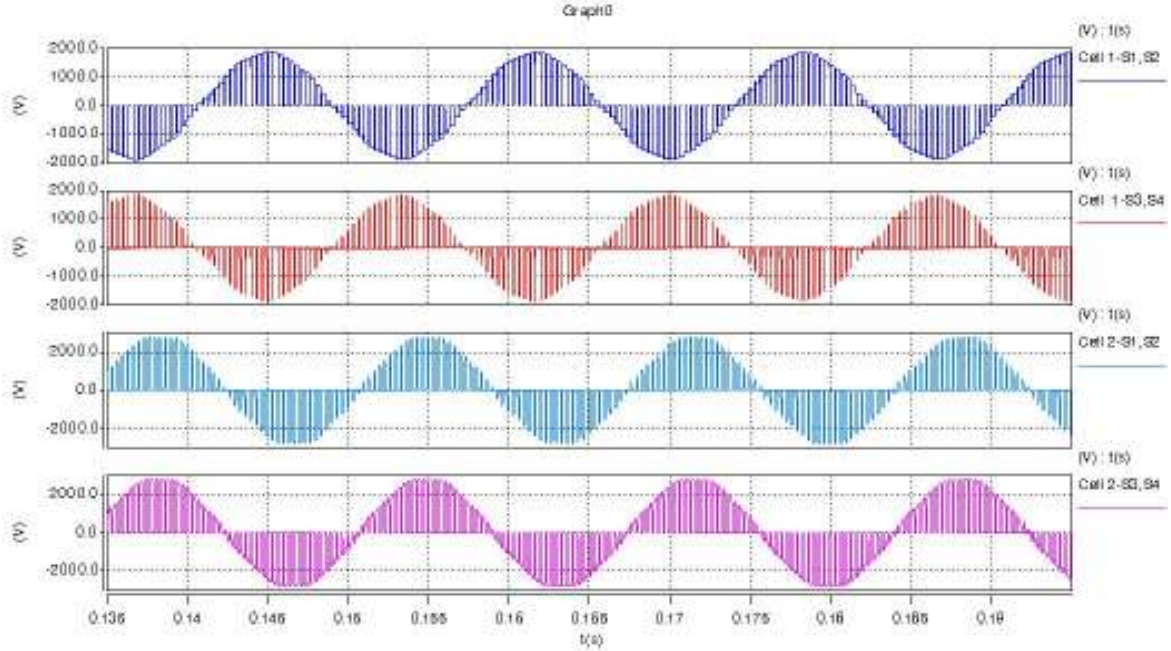
To improve converter operation the boost inductor has been increased. The final value used is 3.1mH. Results illustrating operation of the converter with the modified inductor is shown in Figure 10.27.



(a)



(b)



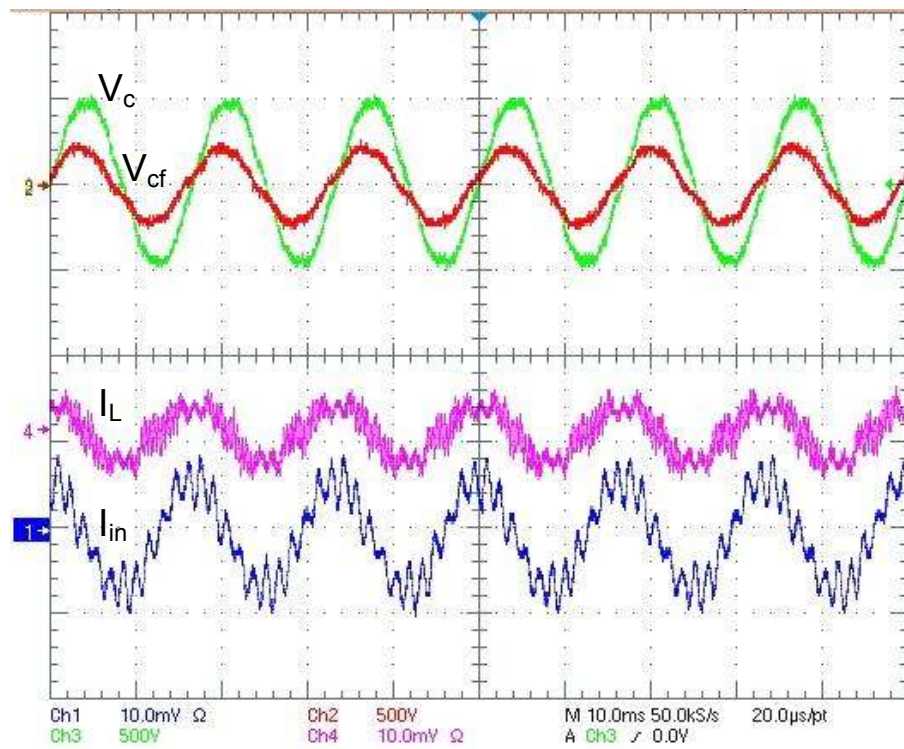
(c)

Figure 10.27: Simulation results for ILSTATCOM at 2400V and 20% boost, (a) V_s , V_{cf} , and V_c , (b) V_s , $5xI_{in}$, I_L , (c) AC switch voltages

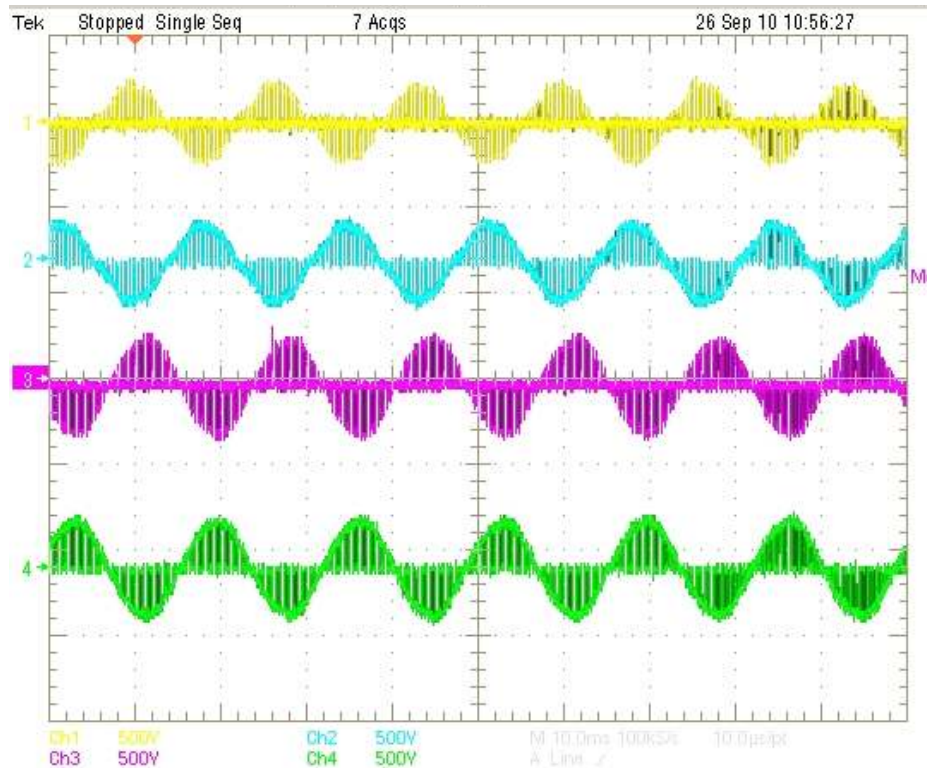
10.7 EXPERIMENTAL RESULTS

Experimental results for the final design of the ILSTATCOM prototype is shown below. The waveforms show operation at an input voltage of 240V and an output voltage of 288V, i.e., voltage across the VAR compensation capacitor. The commutation method used in the final results is voltage and current based commutation with transition between the two modes based on voltage and current information.

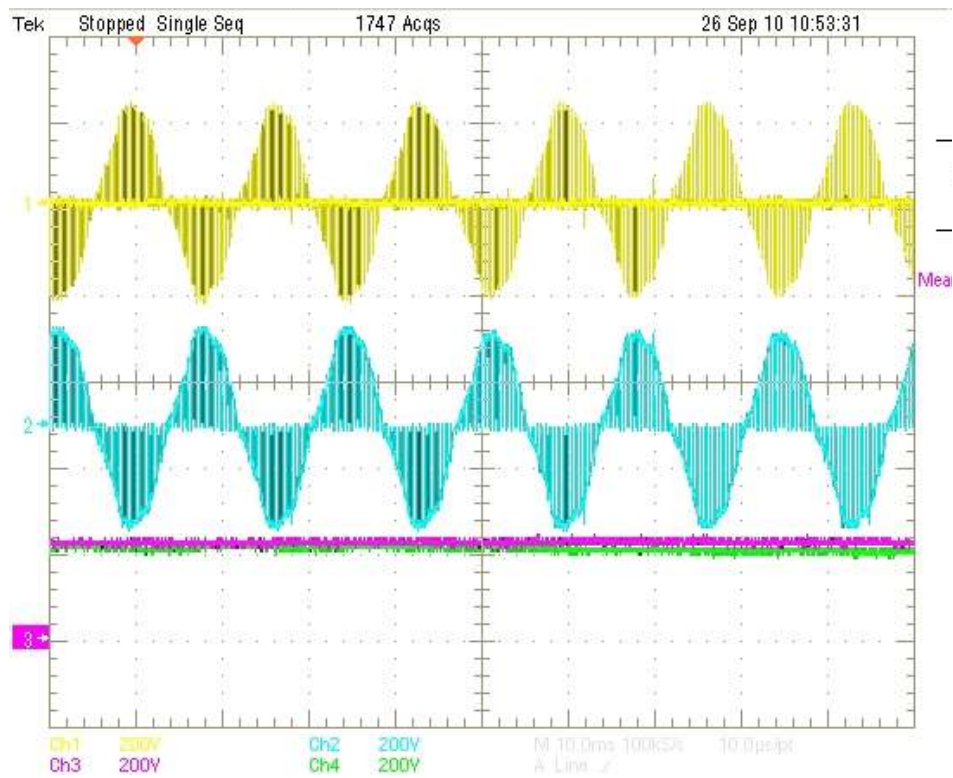
Voltage across the VAR compensation capacitor and filter capacitor is shown in Figure 10.28(a) for an input voltage of 240V. The filter capacitor voltage is controlled to $V_c/2$ and is seen to be phase-shifted with respect to the VAR compensation capacitor voltage. The voltage across the four ac switches is shown in Figure 10.28(b), with details of the four-step commutation switch transitions shown in Figure 10.28(d). The line current and inductor current are shown in Figure 10.28(a). Finally voltage across two AC switches and the snubber voltages for two IGBT's is shown in Figure 10.28(c)



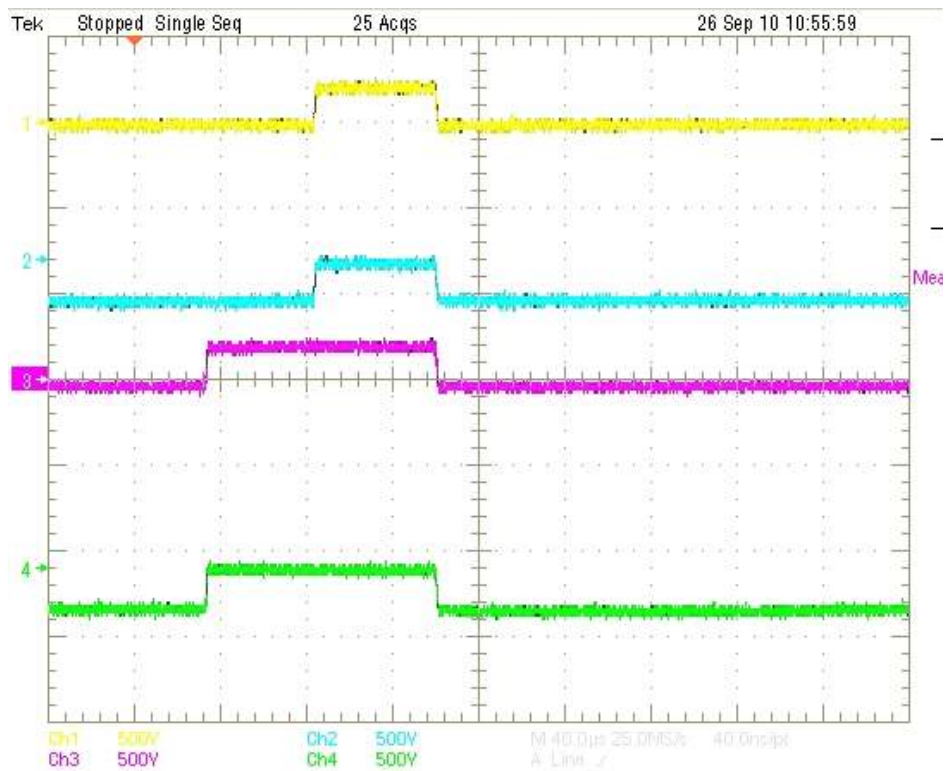
(a)



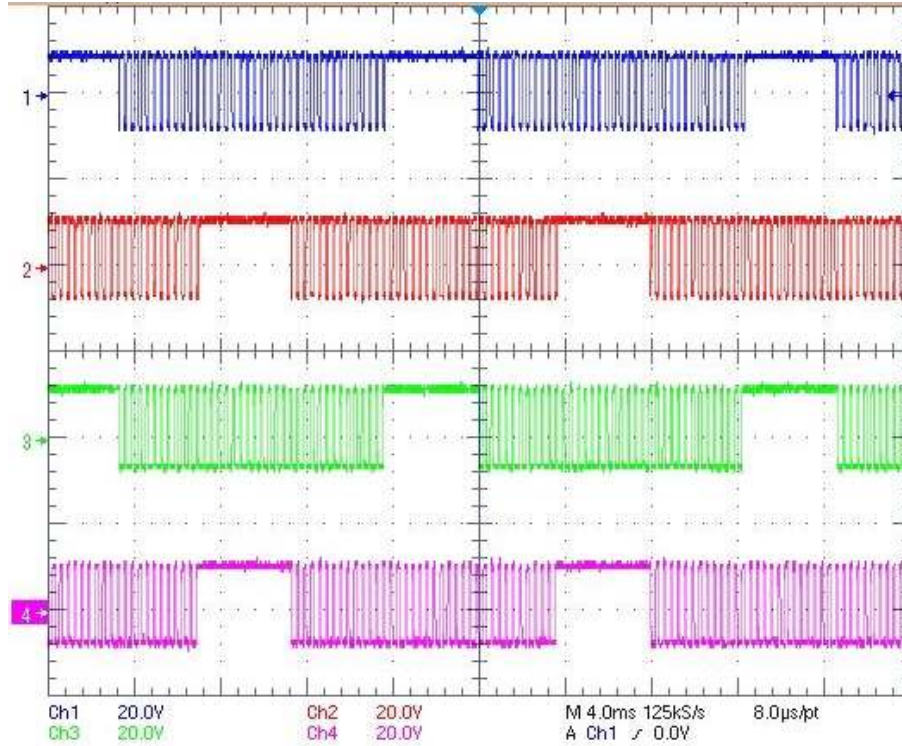
(b)



(c)



(d)



(e)

Figure 10.28: Experimental results for ILSTATCOM at 240V and 20% boost, (a) V_s , V_{cf} , I_L , and I_{in} (b) AC switch voltages, (c) AC switch voltages, snubber voltages, (d) 4-step commutation, (d) gate voltages

Figure 10.28(e) shows the gate voltages for four IGBT's. The voltages have two distinct sections, illustrating the voltage and current commutation regions.

10.8 CONCLUSIONS

Design and implementation of ILSTATOM has been described in this chapter. The design process has been dealt with in detail to demonstrate the level of complexity in the implementation due to factors such as MV IGBT characteristics, AC switch commutation, and component availability, to name a few. The simulation and experimental results validate the design.

CHAPTER 11

CONCLUSIONS AND FUTURE WORK

11.1 CONCLUSIONS

Dynamic control of the existing resources on the power grid can be achieved through the implementation of the concept of thin AC converters. TACCs is a novel idea that provides a method for utilizing existing grid components to realize enhanced dynamic control. The proposed method provides a low-cost solution with high reliability. A TACC is a direct AC-AC converter with no bulk energy storage that is controlled using the concept of virtual quadrature sources (VQS) to enable simultaneous control of multiple variables when implemented on a single-phase basis. The converter is connected to existing resources such as a load tap changing transformer (LTC) or shunt VAR capacitor (SVC) to realize converter-augmented dynamically controllable grid assets. The direct AC-AC converter reflects the asset value on the grid while providing increased dynamic capabilities. A fail-normal mode of operation restores the grid to its original state. This ensures a system has a high reliability at all times.

Control of voltage magnitude and power flow is the primary control objective in a power network. The first can be quite simply achieved by using the direct AC converter with an existing asset (LTC or SVC). The control of phase angle on the grid however requires some form of energy storage. This is a problem due to the cost and complexity associated with adding energy storage to the grid. The principle of virtual quadrature sources provides a novel solution to phase angle and, or harmonic control with no bulk energy storage. Virtual quadrature sources (VQS) is concept that uses voltage synthesis techniques to generate virtual sources that are in quadrature with the line voltage to realize control of the phase angle and, or harmonic components of the voltage or current.

Implementation of this concept using a simple modulation strategy has been shown possible.

The principle of VQS opens up a slew of applications that require conditioning of AC voltages and, or currents. This concept when combined with concept of TACCs results in a novel approach that provides existing grid assets with dynamic control capabilities. Inverter-less active filters and controllable network transformers are two applications that have been presented in some detail. Theoretical analysis as well as simulation and experimental results have been presented for both sets of applications.

Implementing these concepts at realistic voltage and power levels is a critical step in the realization and wide-spread use of this technology. This can be done using a new multilevel direct AC converter that uses low cost off-the-shelf semiconductor devices to realize a high voltage, high power converter. The converter uses an AC chopper as a basic building block to realize a multilevel structure. The converter has been studied in detailed to understand implementation methods, fault modes and limitations. Detailed descriptions of the different fault modes have been included to illustrate the complexities of operation and drawbacks of the converter. Implementation using AC switch commutation techniques has also been presented.

The final application of TACC's considered is the Inverter-less STATCOM (ILSTATCOM). The ILSTATCOM is a dynamic VAR compensator. The device has been simulated to validate the basic concept and also understand system implementation issues. Studies of the impact of multiple ILSTATCOM's in the 13 and 34 node IEEE test systems are presented and compared with conventional VAR compensators, i.e., MSCs and SVCs. The final step in study of the ILSTATCOM is the design and implementation of a medium voltage prototype. The design process has involved electrical, thermal, and mechanical design of the prototype. Individual components have been selected, characterized, and tested to understand component parasitics and possible impact of these parasitics on converter operation. Finally significant work has been done on the commutation techniques for the converter. Novel commutation methods have

been developed specifically for the ILSTATCOM. Simulation and experimental results are presented to validate design and operation of the prototype.

11.2 SUMMARY OF CONTRIBUTIONS

The following is a summary of contributions.

11.2.1 CONCEPT OF THIN AC CONVERTERS

The concept of TACCs has been proposed as part of this research. This concept is an invaluable asset in realizing increased dynamic control using existing grid components. The TACC is a direct AC converter with small L, C filter components and no bulk energy storage. The most important advantages of this concept are the fail-normal mode of operation, and utilization of the grid asset as the bulk energy storage component at the fundamental frequency. This ensures both high reliability and low-cost. TACCs are implemented on a single-phase basis and are fractionally rated converters that provide vernier control. These devices are distributed in the network close to or at the points where control is required.

11.2.2 PRINCIPLE OF VIRTUAL QUADRATURE SOURCES

The principle of VQSs is a novel concept in AC power conversion. VQSs enables the control of phase angle and, or harmonic components of an AC voltage or current with no energy storage. This is not possible with conventional techniques. The principle of VQSs proposes a fundamental technique that enables the shuffling of energy between quadrature sources at different frequencies to realize the desired output. The basic idea has been proposed, presented, and validated using analysis and simulations. Experimental verification has also been presented. The concept is vital in the realization of TACCs and also expands the range of applications for TACCs.

11.2.3 MULTILEVEL DIRECT AC CONVERTER

Scaling the TACC has been addressed with a novel direct AC converter topology. The proposed converter uses an AC chopper as a basic building block to realize a cascaded topology that is similar in structure to a flying capacitor converter. Detailed analysis of the operating modes, snubber requirements, and commutation method has been presented. Converter operation has been verified using simulations and experimentally.

11.2.4 APPLICATIONS – CNT, ILSTATCOM, ACTIVE FILTERS

Three applications for the TACC concept have been proposed. The CNT is a device that provides simultaneous control of voltage magnitude and phase angle. The device uses the concept of VQS to provide control on a single-phase basis with no energy storage. The basic principle has been studied in a four-bus system. Autonomous control has been tested using an algorithm based on a simplified model that has been developed for the device.

ILSTATCOMs provide dynamic VAR compensation. The device is a converter-augmented VAR compensation capacitor. The ILSTATCOM is made up of buck and boost cells that reflect the bucked or boosted capacitance on the grid.

The third application proposed is active filters. The principle of VQS provides a method to control harmonics with no energy storage. This control handle is leveraged to realize active filtering functions. Resistive, inductive, and capacitive cells have been proposed. Validation of the basic concept is presented with simulation and experimental results.

11.2.5 DESIGN AND IMPLEMENTATION OF A MV ILSTATCOM

The proposed concepts have been validated through the design and implementation of a MV TACC device. The application considered is the ILSTATCOM. This task is a significant step in the validation of TACCs, as it brings to light issues with the actual implementation. Each component of the converter has been designed and characterized. The design process has been iterative as issues at every stage have been resolved through revisions.

11.2.6 COMMUTATION METHODS

Commutation methods have been developed for the operation of the multilevel direct AC converter, specifically the ILSTATCOM. The methods developed have been a significant part of the implementation process at every stage, and hence are considered a worthy contribution of this thesis. Each method has been verified and tested both in simulation and experimentally.

11.3 RECOMMENDATIONS FUTURE WORK

The following tasks have been identified as avenues for future work based on the contributions of this dissertation.

1. Control algorithms for multiple distributed ILSTATCOMs in a system.
2. Intelligent gate drives for safe commutation
3. Improved snubber topology to eliminate transients
4. Consider scaling using series connection of devices and multilevel topology.

11.3.1 CONTROL OF MULTIPLE DISTRIBUTED ILSTATCOM'S IN A SYSTEM

Control of multiple distributed devices has been researched extensively. This specific task would aim at developing a simple control algorithm to enable local control of distributed devices to ensure system-wide benefit of these devices. Consider a single ILSTATCOM connected to a distribution network. Control of the single device is quite trivial, as simple voltage and, or current measurements can be used in a closed-loop control algorithm. If there are multiple devices connected to the same distribution feeder the control set-points for power factor correction can be determined using localized measurements. For control of the voltage profile of the feeder, the set-points for each device would have to be determined based on local and global measurements. One way to do this is develop a sensitivity matrix of the feeder, which is an indication of geographical proximity, to determine the impact of devices at different points on the feeder.

11.3.2 INTELLIGENT GATE DRIVES FOR SAFE COMMUTATION

Commutation of AC switches has been dealt with in a lot of detail for the implementation of the multilevel direct AC converter, specifically in the implementation of the ILSTATCOM prototype. Significant improvement can be made in the commutation technique if the state machine is localized, i.e. state machine is designed per device, at the gate drive level. Further improvement in device commutation can be made with intelligent control of device switching.

11.3.3 IMPROVED SNUBBER TOPOLOGY TO ELIMINATE TRANSIENTS

The snubber used in the implementation of the direct AC converter is designed to be a safety-net in case of bad commutation and fault modes. The snubber however is configured to regulate a DC voltage across the capacitor because of the charging and discharging paths created by the diode and resistor respectively. Because of the DC voltage across the snubber capacitor the effect of all transients, while contained by the snubber, are seen across the filter and VAR compensation capacitor. Significant improvements can be made in the snubber topology and design to eliminate these issues.

11.3.4 SCALING METHODS

Scaling for the TACC concept has been addressed by the multilevel direct AC converter topology. There are however limitations to the use of this topology. The number of levels is limited because of the control headroom available for voltage regulation across the different cells. Also, the use of high voltage IGBT's has repercussions on the filter sizes, i.e., the low switching frequency of these devices results in increased filter size requirements. An optimal way to therefore implement this concept would be to series connect low voltage IGBT's that would increase the voltage rating of each cell, thereby limiting the number of levels required by the converter.

11.4 LIST OF PUBLICATIONS

The following is a list of publications that has resulted from the work presented in this dissertation.

- Deepak Divan, Jyoti Sastry, “ Voltage Synthesis Using Dual Virtual Quadrature Sources – A New Concept in AC Power Conversion”, IEEE Transaction on Power Electronics, Vol. 23, No. 6, November 2008, pp. 3004 – 3013.
- Deepak Divan, Jyoti Sastry, “Inverter-Less Active Filters – A New Concept in VAR and Harmonic Compensation”, IEEE Power Electronics Specialists Conference (PESC), June 2007. pp. 2926-2932.
- Jyoti Sastry, Deepak Divan “Controllable Network Transformers”, IEEE Power Electronics Specialists Conference (PESC), June 2008. pp. 2340-2345.
- Deepak Divan, Jyoti Sastry “Inverter-less STATCOMs”, IEEE Power Electronics Specialists Conference (PESC), June 2008. pp. 1372-1377.
- Deepak Divan, Jyoti Sastry, Anish Prasai, Harjeet Johal, “Thin AC Converters – A New Approach to Making Grid Assets Smart and Controllable”, IEEE Power Electronics Specialists Conference (PESC), June 2008. pp. 1695-1701.
- Jyoti Sastry, Deepak Divan “Control of Multilevel Direct AC Converters”, IEEE Energy Conversion Congress and Exposition (ECCE) 2009, September 2009.

APPENDIX A

IEEE 13 NODE FEEDER DATA

Overhead Line Configuration Data:

Config.	Phasing	Phase	Neutral	Spacing
		ACSR	ACSR	ID
601	B A C N	556,500 26/7	4/0 6/1	500
602	C A B N	4/0 6/1	4/0 6/1	500
603	C B N	1/0	1/0	505
604	A C N	1/0	1/0	505
605	C N	1/0	1/0	510

Underground Line Configuration Data:

Config.	Phasing	Cable	Neutral	Space ID
606	A B C N	250,000 AA, CN	None	515
607	A N	1/0 AA, TS	1/0 Cu	520

Line Segment Data:

Node A	Node B	Length(ft.)	Config.
632	645	500	603
632	633	500	602
633	634	0	XFM-1
645	646	300	603
650	632	2000	601
684	652	800	607
632	671	2000	601
671	684	300	604
671	680	1000	601
671	692	0	Switch
684	611	300	605
692	675	500	606

Transformer Data:

	kVA	kV-high	kV-low	R - %	X - %
Substation:	5,000	115 - D	4.16 Gr. Y	1	8
XFM -1	500	4.16 – Gr.W	0.48 – Gr.W	1.1	2

Capacitor Data:

Node	Ph-A	Ph-B	Ph-C
	kVAr	kVAr	kVAr
675	200	200	200
611			100
Total	200	200	300

Regulator Data:

Regulator ID:	1		
Line Segment:	650 - 632		
Location:	50		
Phases:	A - B -C		
Connection:	3-Ph,LG		
Monitoring Phase:	A-B-C		
Bandwidth:	2.0 volts		
PT Ratio:	20		
Primary CT Rating:	700		
Compensator Settings:	Ph-A	Ph-B	Ph-C
R - Setting:	3	3	3
X - Setting:	9	9	9
Voltage Level:	122	122	122

Spot Load Data:

Node	Load	Ph-1	Ph-1	Ph-2	Ph-2	Ph-3	Ph-3
	Model	kW	kVAr	kW	kVAr	kW	kVAr
634	Y-PQ	160	110	120	90	120	90
645	Y-PQ	0	0	170	125	0	0
646	D-Z	0	0	230	132	0	0
652	Y-Z	128	86	0	0	0	0
671	D-PQ	385	220	385	220	385	220
675	Y-PQ	485	190	68	60	290	212
692	D-I	0	0	0	0	170	151

611	Y-I	0	0	0	0	170	80
	TOTAL	1158	606	973	627	1135	753

Distributed Load Data:

Node A	Node B	Load	Ph-1	Ph-1	Ph-2	Ph-2	Ph-3	Ph-3
		Model	kW	kVAr	kW	kVAr	kW	kVAr
632	671	Y-PQ	17	10	66	38	117	68

IEEE 34 NODE FEEDER DATA

Line Segment Data:

Node A	Node B	Length(ft.)	Config.
800	802	2580	300
802	806	1730	300
806	808	32230	300
808	810	5804	303
808	812	37500	300
812	814	29730	300
814	850	10	301
816	818	1710	302
816	824	10210	301
818	820	48150	302
820	822	13740	302
824	826	3030	303
824	828	840	301
828	830	20440	301
830	854	520	301
832	858	4900	301
832	888	0	XFM-1
834	860	2020	301
834	842	280	301
836	840	860	301
836	862	280	301
842	844	1350	301
844	846	3640	301
846	848	530	301
850	816	310	301
852	832	10	301
854	856	23330	303
854	852	36830	301
858	864	1620	303
858	834	5830	301
860	836	2680	301
862	838	4860	304
888	890	10560	300

Overhead Line Configurations

Config.	Phasing	Phase	Neutral	Spacing ID
		ACSR	ACSR	
300	B A C N	1/0	1/0	500
301	B A C N	#2 6/1	#2 6/1	500
302	A N	#4 6/1	#4 6/1	510
303	B N	#4 6/1	#4 6/1	510
304	B N	#2 6/1	#2 6/1	510

Transformer Data

	kVA	kV-high	kV-low	R - %	X - %
Substation:	2500	69 - D	24.9 - Gr. W	1	8
XFM -1	500	24.9 - Gr.W	4.16 - Gr. W	1.9	4.08

Spot Loads

Node	Load	Ph-1	Ph-2	Ph-3	Ph-4
	Model	kW	kVAr	kW	kVAr
860	Y-PQ	20	16	20	16
840	Y-I	9	7	9	7
844	Y-Z	135	105	135	105
848	D-PQ	20	16	20	16
890	D-I	150	75	150	75
830	D-Z	10	5	25	10
Total		344	224	344	229

Distributed Loads

Node	Node	Load	Ph-1	Ph-2	Ph-3	Ph-3
A	B	Model	kW	kVAr	kW	kVAr
802	806	Y-PQ	0	0	30	15
808	810	Y-I	0	0	16	8
818	820	Y-Z	34	17	0	0
820	822	Y-PQ	135	70	0	0
816	824	D-I	0	0	5	2
824	826	Y-I	0	0	40	20
824	828	Y-PQ	0	0	0	4
828	830	Y-PQ	7	3	0	0
854	856	Y-PQ	0	0	4	2
832	858	D-Z	7	3	2	1
858	864	Y-PQ	2	1	0	0
858	834	D-PQ	4	2	15	8
834	860	D-Z	16	8	20	10
860	836	D-PQ	30	15	10	6
836	840	D-I	18	9	22	11
862	838	Y-PQ	0	0	28	14
842	844	Y-PQ	9	5	0	0
844	846	Y-PQ	0	0	25	12
846	848	Y-PQ	0	0	23	11
Total			262	133	240	120

Shunt Capacitors

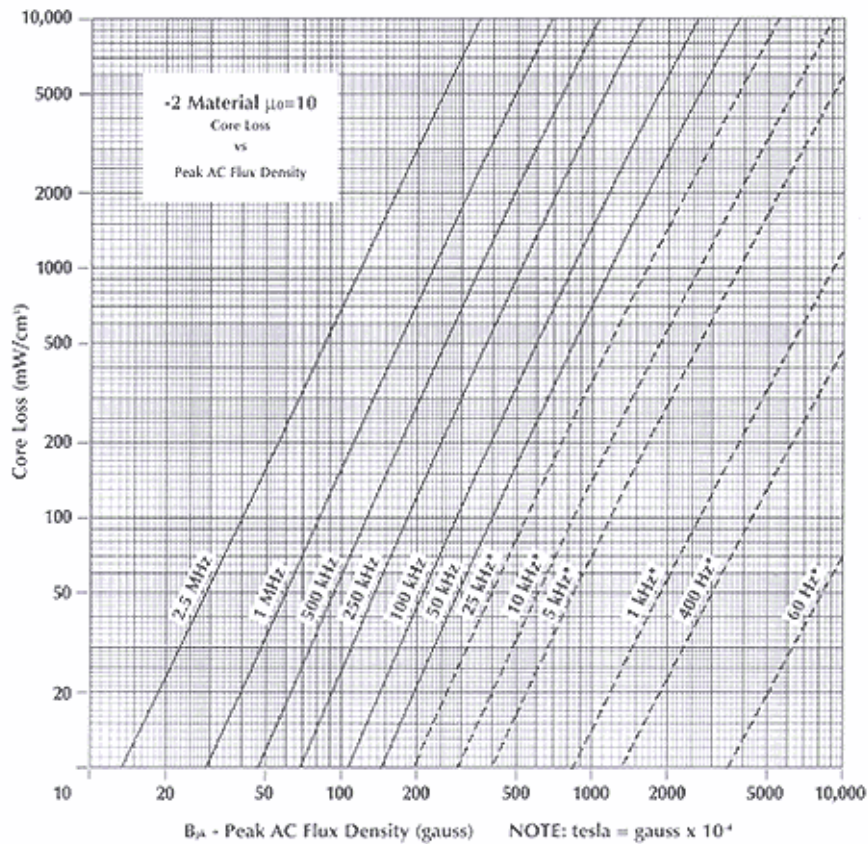
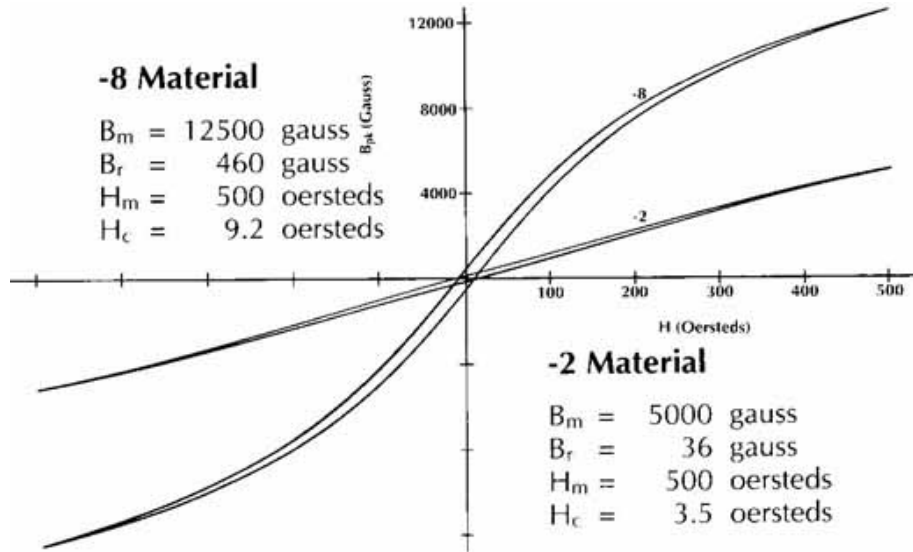
Node	Ph-A	Ph-B	Ph-C
	kVAr	kVAr	kVAr
844	100	100	100
848	150	150	150
Total	250	250	250

Regulator Data

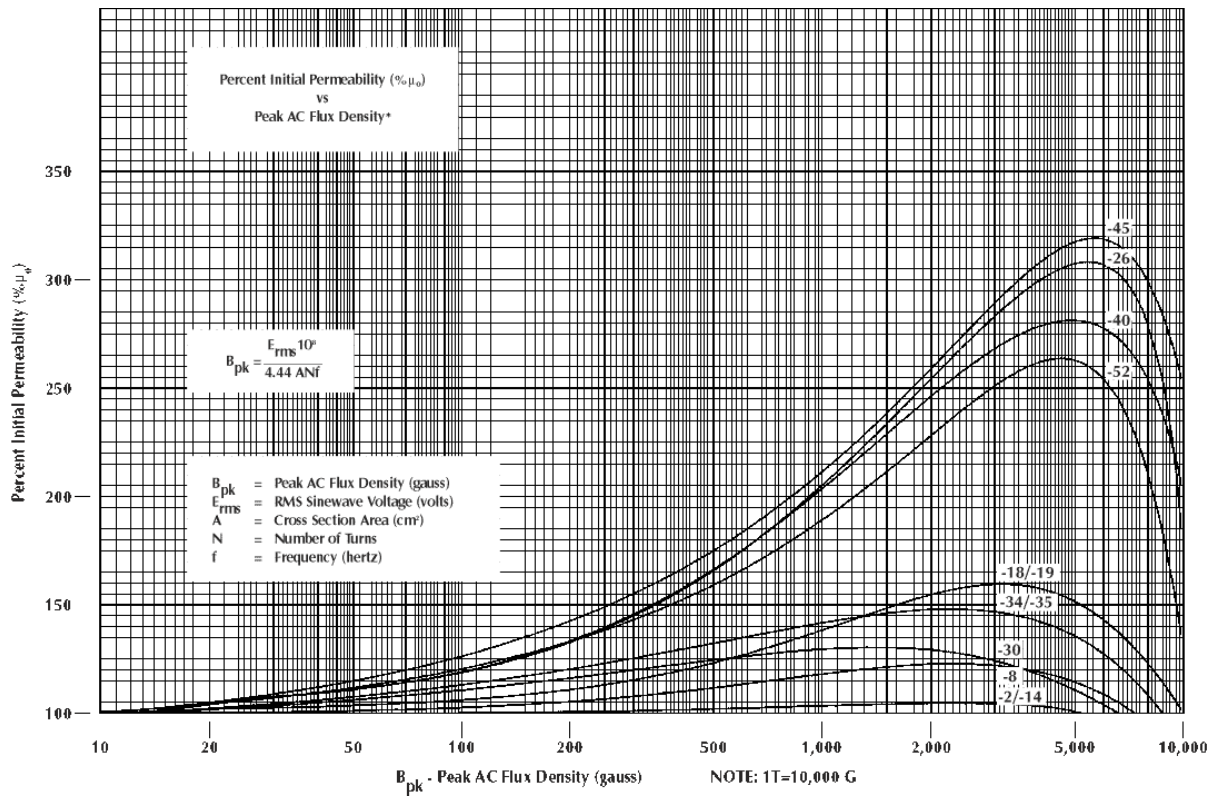
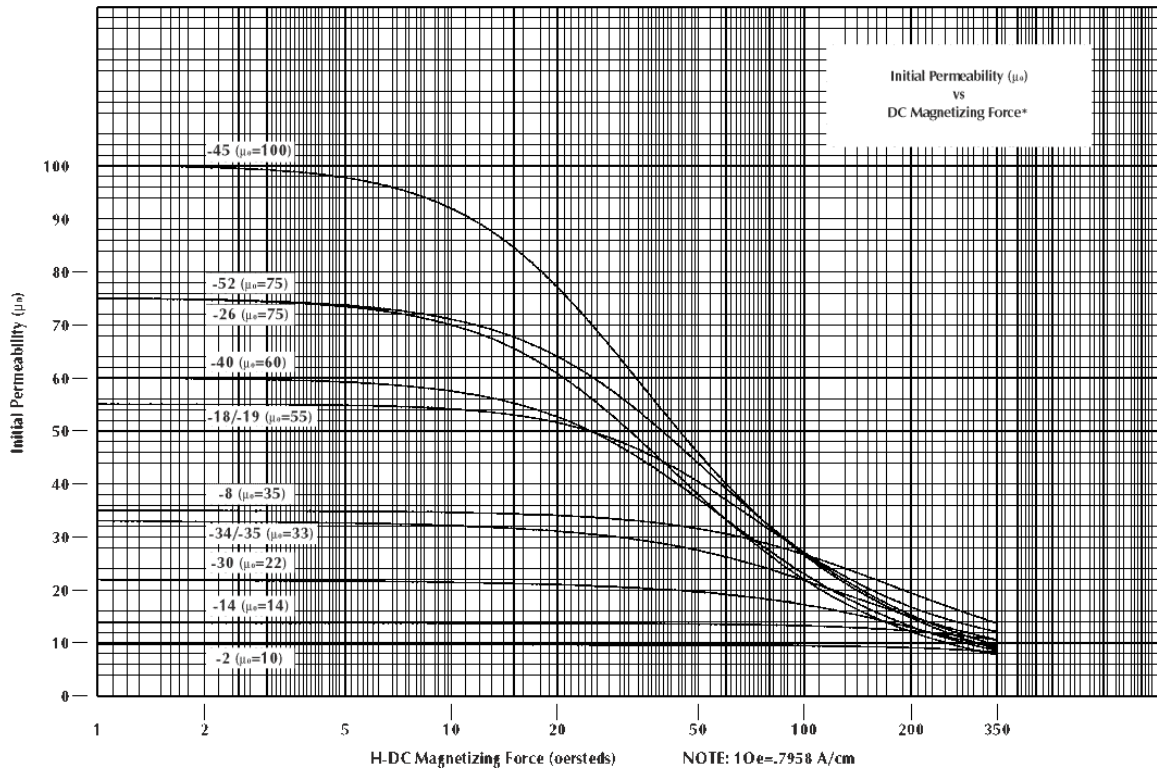
Regulator ID:	1		
Line Segment:	814 - 850		
Location:	814		
Phases:	A - B -C		
Connection:	3-Ph,LG		
Monitoring Phase:	A-B-C		
Bandwidth:	2.0 volts		
PT Ratio:	120		
Primary CT Rating:	100		
Compensator Settings:	Ph-A	Ph-B	Ph-C
R - Setting:	2.7	2.7	2.7
X - Setting:	1.6	1.6	1.6
Voltage Level:	122	122	122
Regulator ID:	2		
Line Segment:	852 - 832		
Location:	852		
Phases:	A - B -C		
Connection:	3-Ph,LG		
Monitoring Phase:	A-B-C		
Bandwidth:	2.0 volts		
PT Ratio:	120		
Primary CT Rating:	100		
Compensator Settings:	Ph-A	Ph-B	Ph-C
R - Setting:	2.5	2.5	2.5
X - Setting:	1.5	1.5	1.5
Voltage Level:	124	124	124

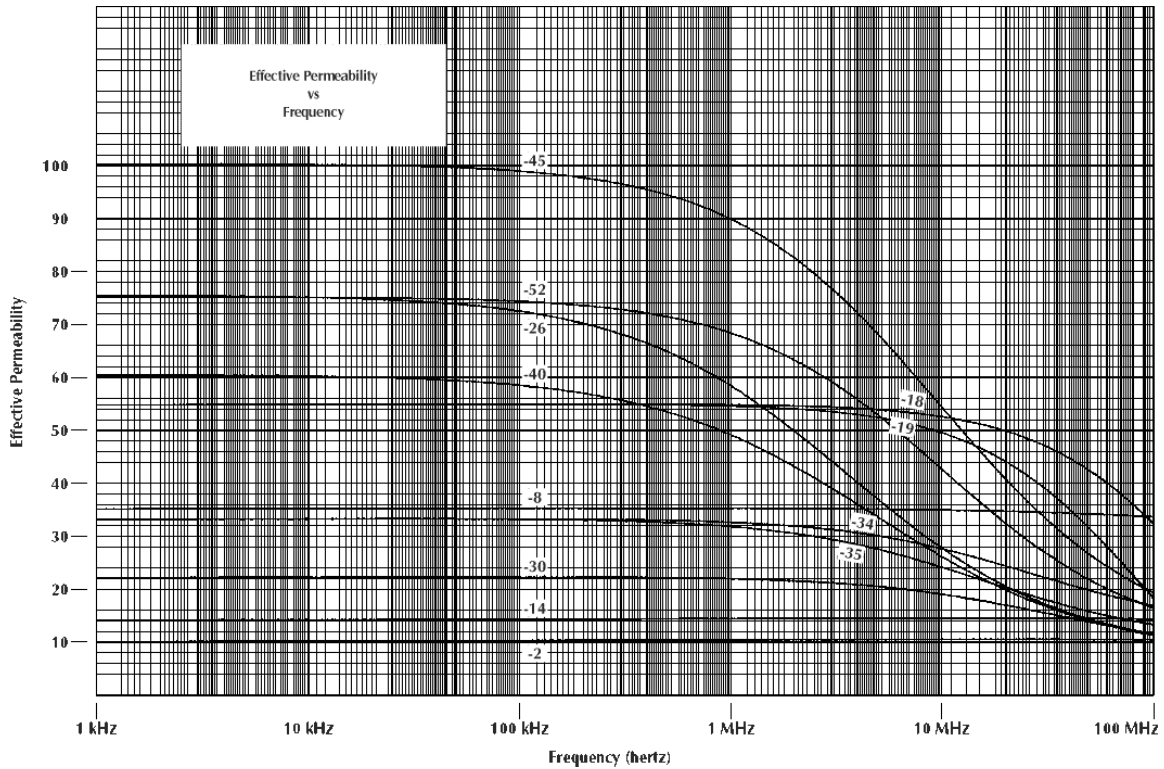
APPENDIX B

CORE PROPERTIES - Micrometals -2



*Low frequency core loss is extrapolated from data measured at high frequency.





PERCENT PERMEABILITY vs DC MAGNETIC FORCE*

FORMULA: $\%m = ((a+cH+eH^2)/(1+bH+dH^2))^{1/2}$

Where: $\%m$ = Percentage (ie: 90%=90)
H = DC Magnetizing Force (oersteds)

Material	a	b	c	d	e
-2**	10000	6.13×10^{-4}	5.22	3.51×10^{-6}	4.64×10^{-3}
-14**	10000	5.61×10^{-4}	5.05	6.86×10^{-6}	5.58×10^{-3}
-8	10090	4.26×10^{-3}	30.9	7.68×10^{-5}	-.0119
-18/-19	9990	8.36×10^{-4}	14.4	3.92×10^{-4}	.0853
-26	10090	5.05×10^{-3}	13.1	1.17×10^{-3}	.0212
-30	10140	4.68×10^{-4}	-30.2	1.45×10^{-5}	.0505
-34/-35	10200	5.12×10^{-3}	7.39	9.62×10^{-5}	.0298
-40	10240	4.32×10^{-3}	12.8	6.26×10^{-4}	.0267
-45	10014	6.07×10^{-3}	45.2	1.79×10^{-3}	-.0578
-52	10240	6.71×10^{-3}	24.7	7.75×10^{-4}	-.0105

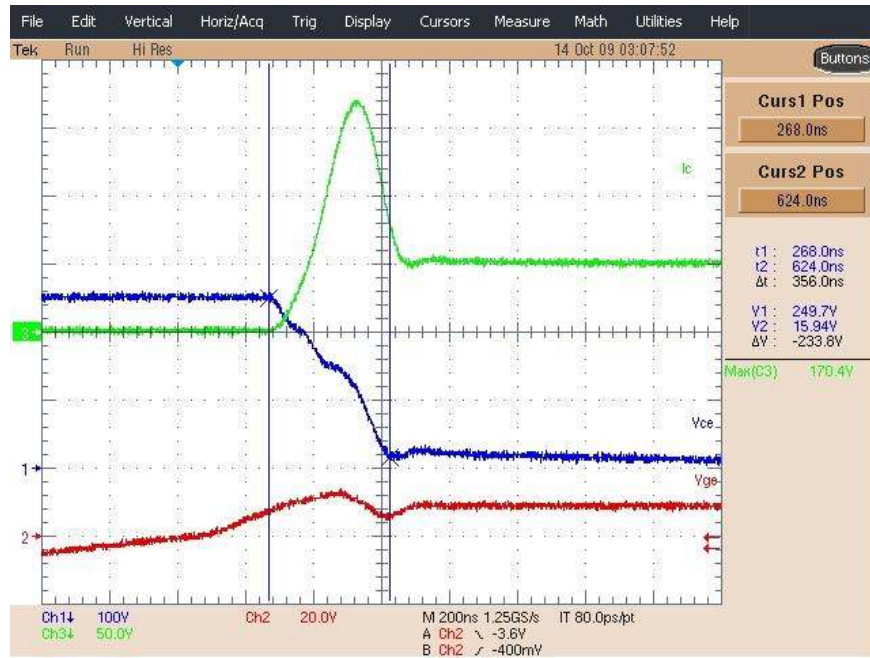
* Curve fit formula valid only for ranges shown on graph

APPENDIX C

RESULTS OF DEVICE CHARACTERIZATION

The following Table shows the results of the device characterization setup. Plots corresponding to the results are included.

DC bus voltage Vdc	252V
Steady state current Ic	50.7A
<i>Image Number</i>	Figure 1(a)
Current rise time (ns)	84
Reverse recovery time (ns)	284
Peak reverse recovery current (A)	170.4
Turn on Delay (ns)	164
Vce fall to Vce sat	356ns, 1.08us
Vce Sat (V)	Drops from 6.3V to 5V
Turn on Switching Loss (Joules)	4.765m
Ratio (V*I/Loss)	2.59706191
Conduction Loss (Watts)	616
SS Current immediately before second turn off	54.4A
<i>Image Number</i>	Figure 1(b)
Current fall time (ns)	1.62us
Vce rise time	620ns, 254ns
Vce peak during ringing (V)	285.3
Turn off delay time (us)	1.48us
Turn off switching loss (Joules)	16.61m
Ratio (V*I/Loss)	0.808549067
Pulse widths (us)	58.64us, 156.08us, 8.24us
Command	T016,045,001,P
Miscellaneous	Vge = +15V/-9.5V



(a)



(b)

Figure 1: Results for IGBT characterization, 252V, 50A

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